



WELCOME To

**ISSCC 2014
SESSION 4
DC-DC
CONVERTERS**

A 3-Phase Digitally Controlled DC-DC Converter with 88% Ripple Reduced 1-Cycle Phase Adding/Dropping Scheme and 28% Power Saving CT/DT Hybrid Current Control

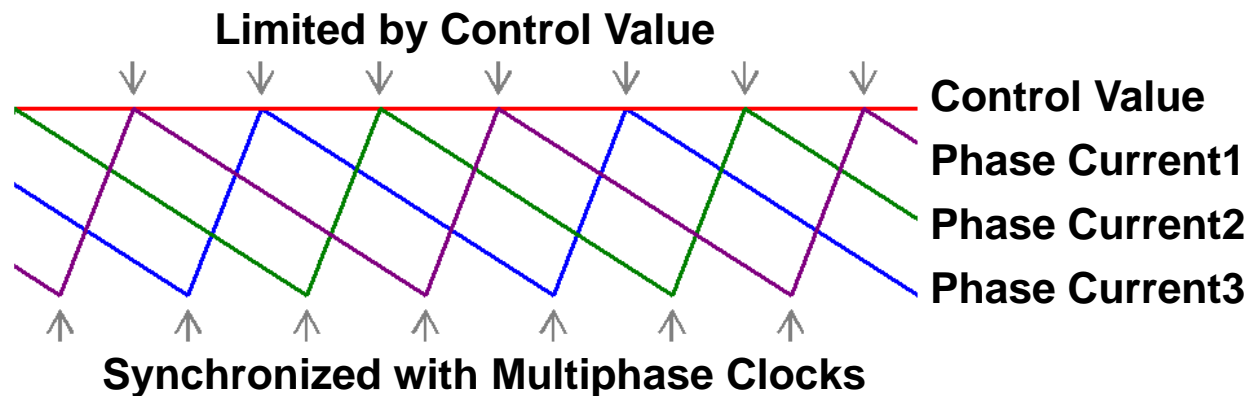
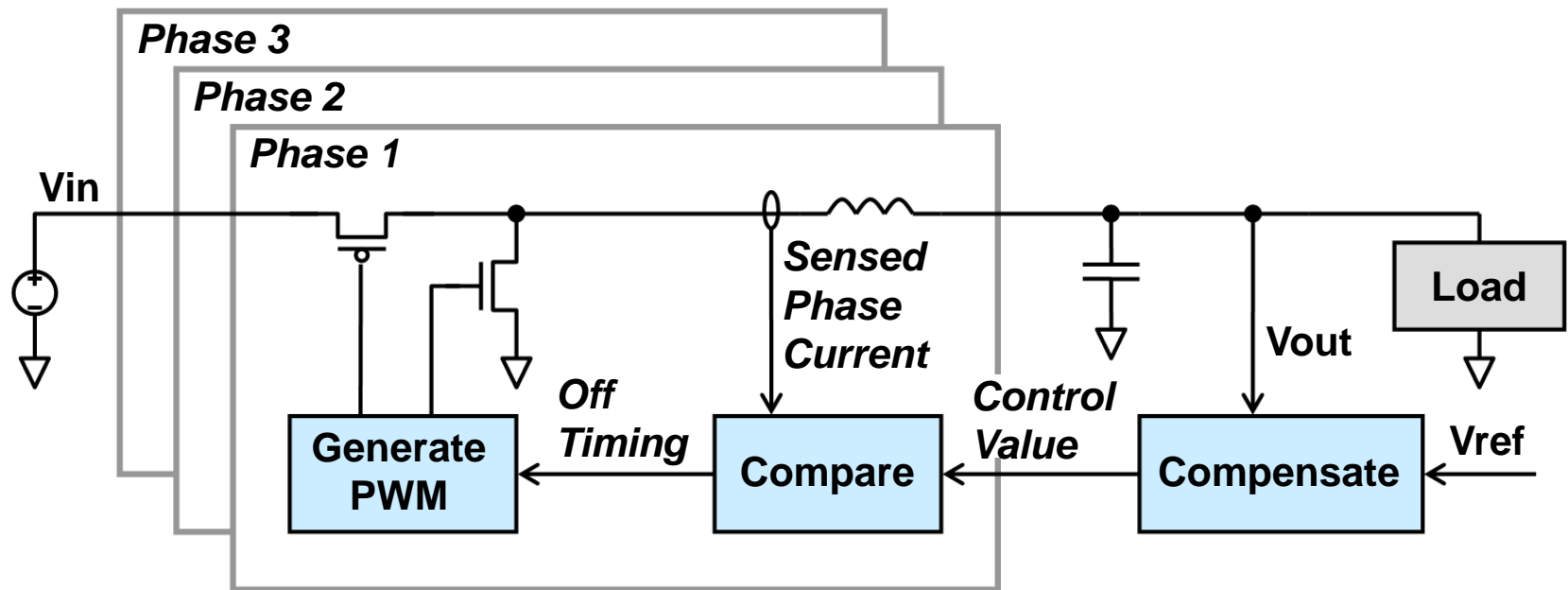
Chen Kong TEH,
Atsushi SUZUKI, Manabu YAMADA,
Mototsugu HAMADA, Yasuo UNEKAWA

Toshiba Corporation
Kawasaki, Japan

Outline

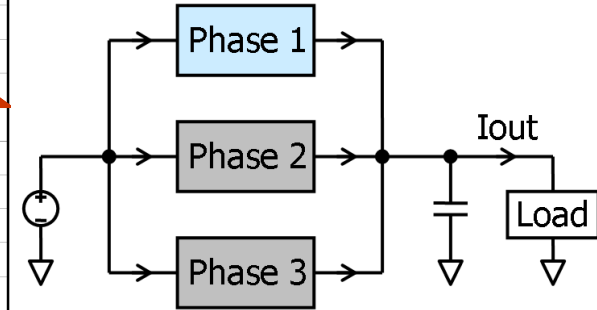
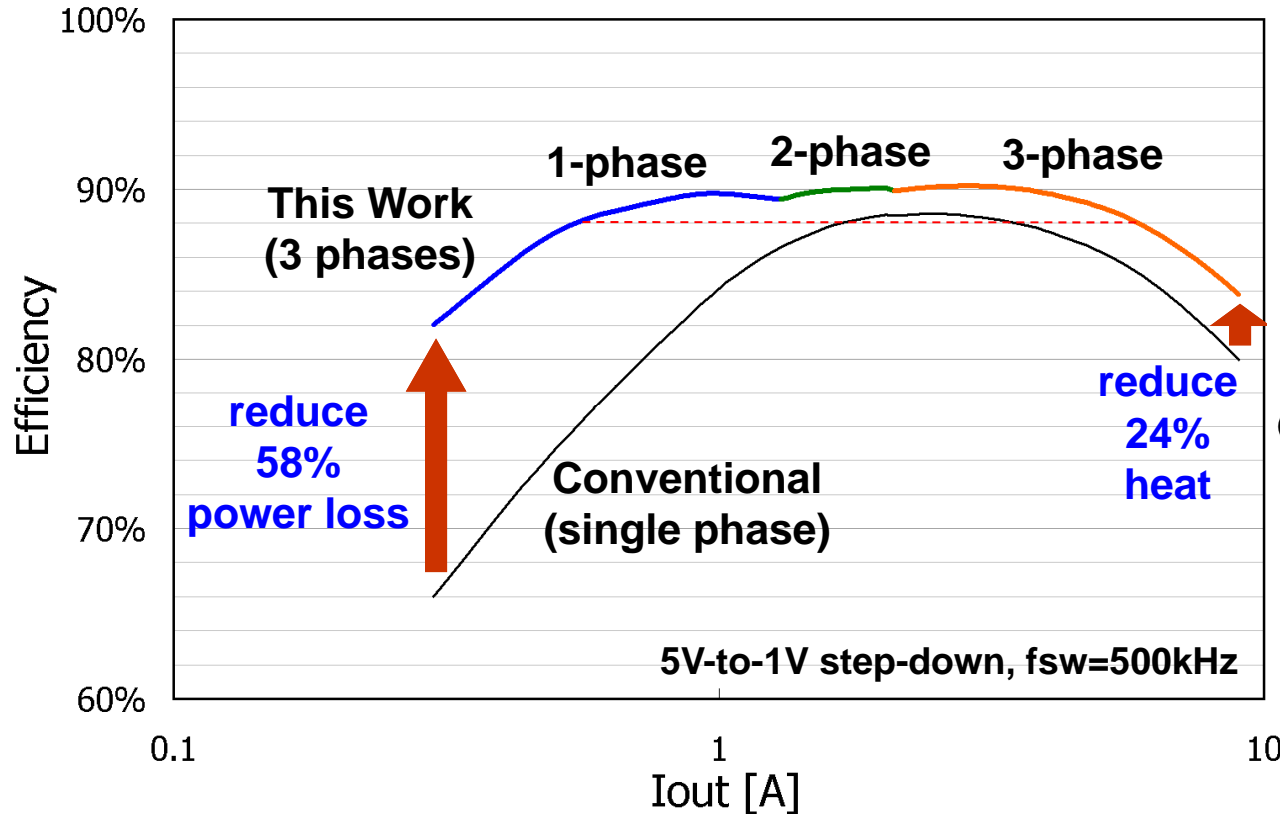
- **Motivation**
- **Proposed Architecture**
 - **Phase Adding/Dropping Scheme**
 - **CT/DT Hybrid Current Control**
 - **Fast Transient Response Configuration**
- **Measured Results**
- **Summary**

Introduction: Multiphase Topology



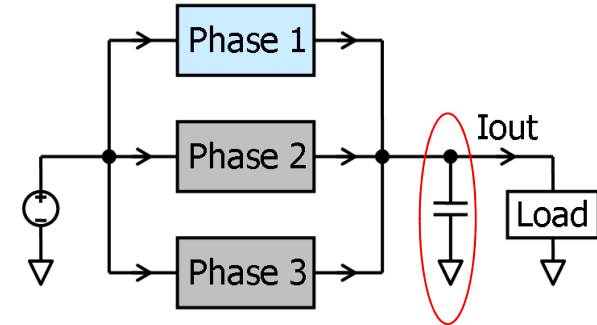
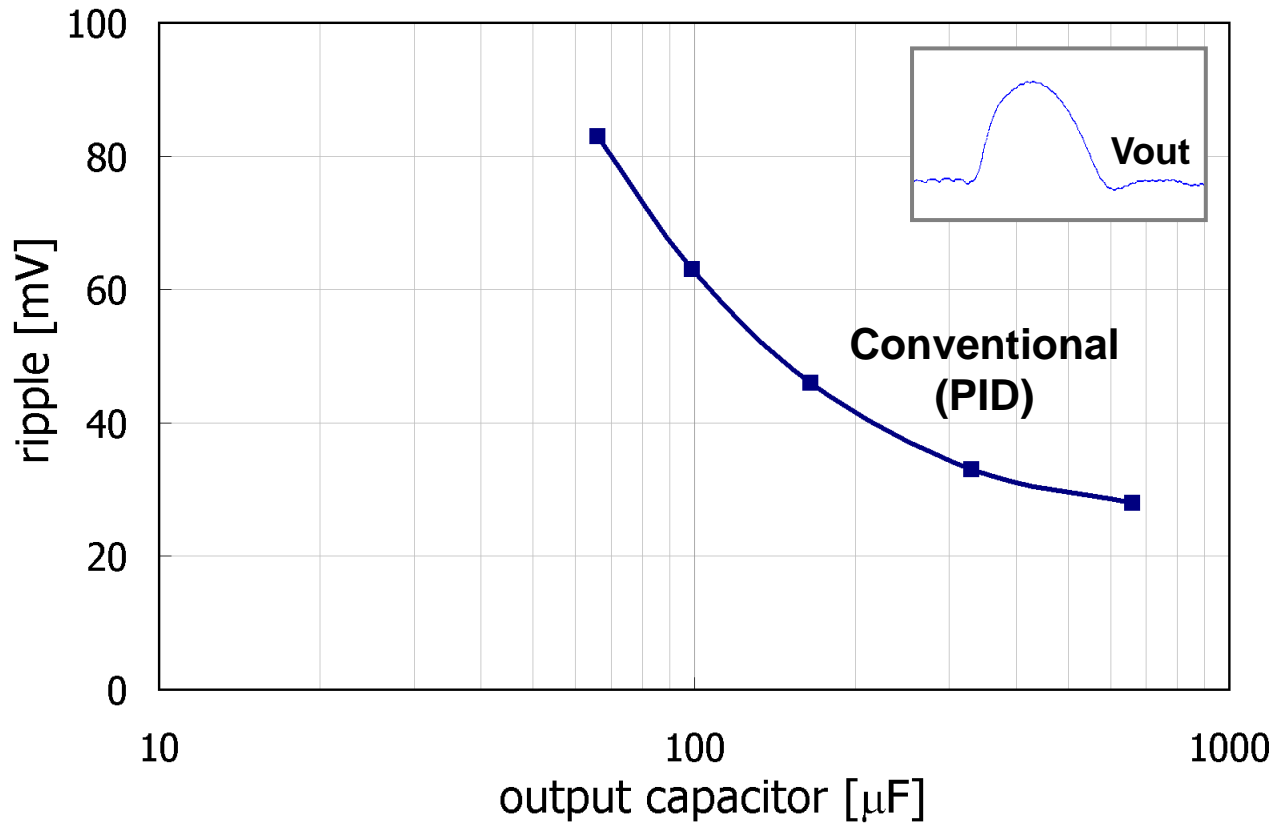
Deliver load current by several parallel phases (units).

Motivation



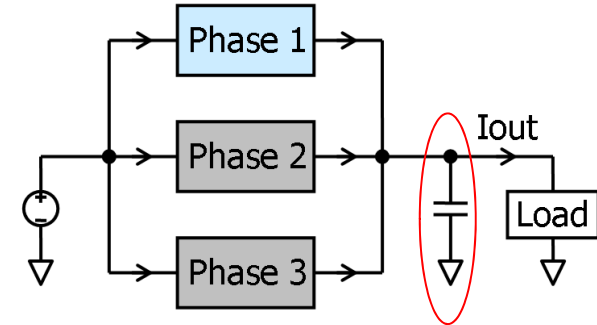
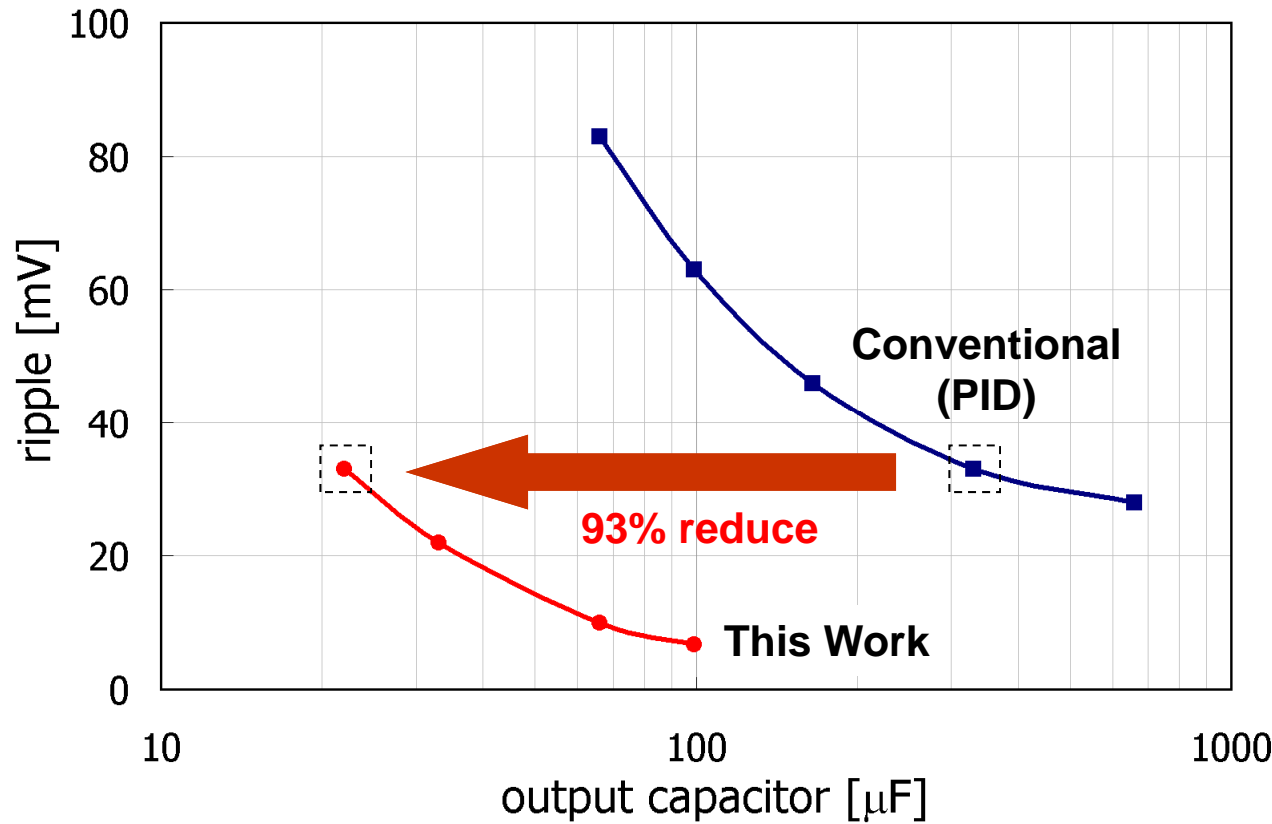
- Today's mobile devices utilize multicore designs that have a wide range of current profile.
- Require DC-DC converters with a good efficiency over a wide range of load.
- Use multiphase topology with the number of active phases adjusted according to load conditions.

Challenge



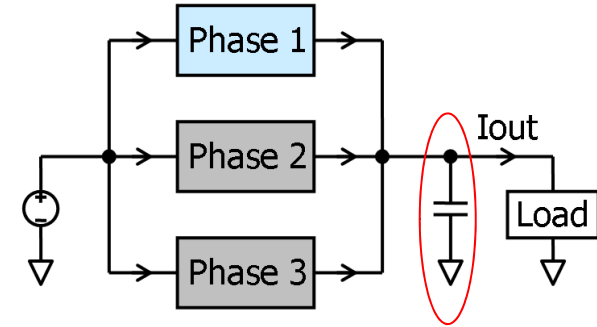
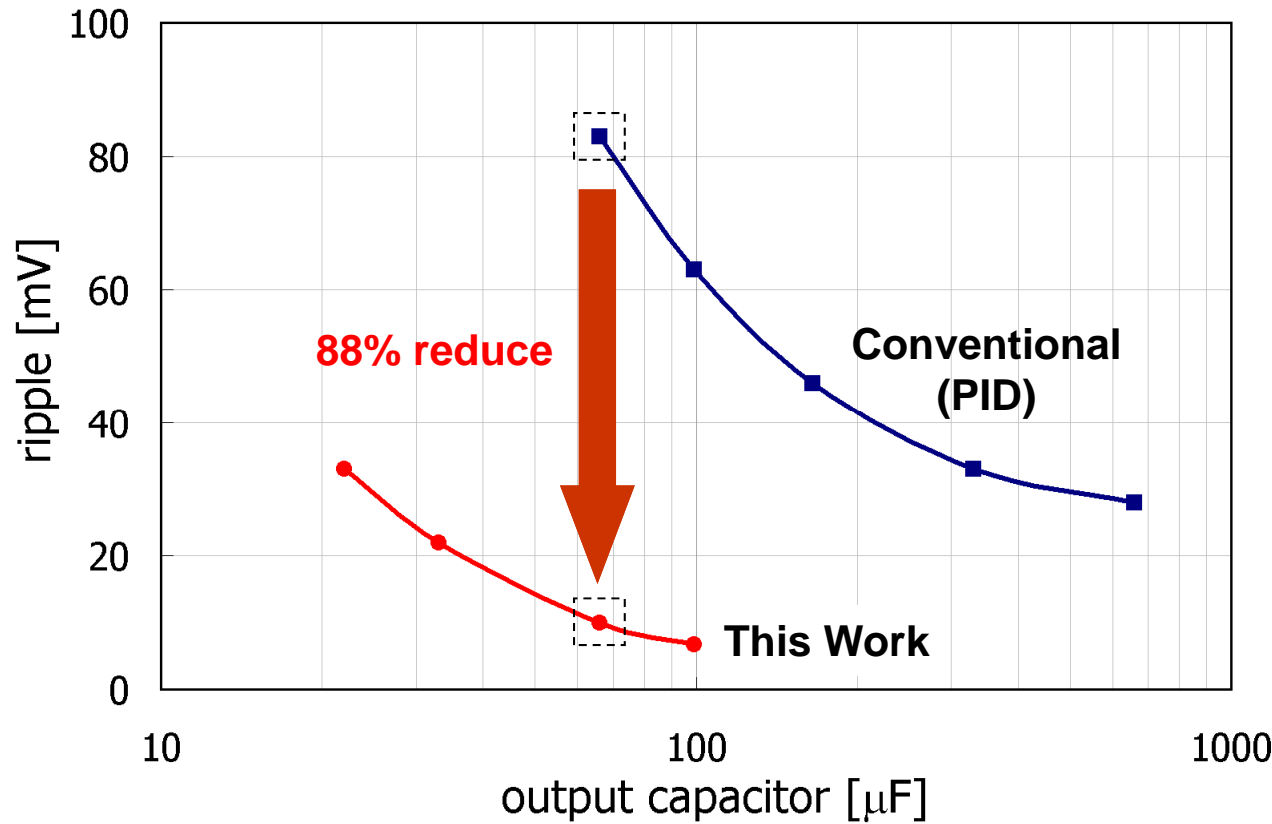
- **Active-phase-count transition induces a large ripple.**
- **Conventional solutions require large output capacitors to counter the ripple.**
- **Phase adding/dropping scheme is proposed for mobile devices.**

Challenge



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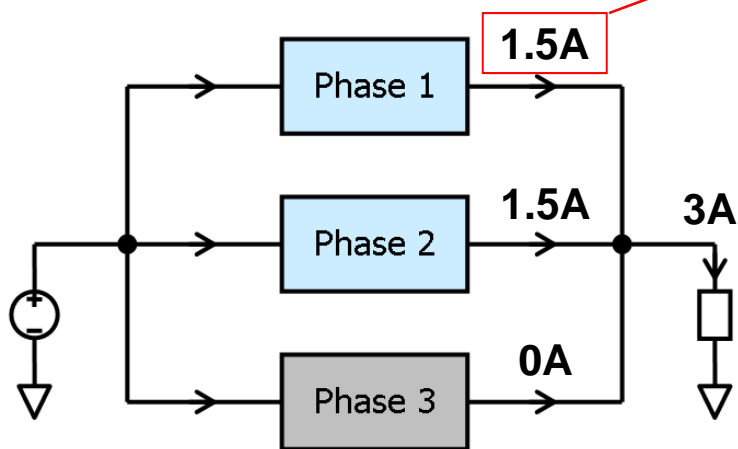
Concept

- How to achieve a nearly optimal response?
 - Design a **non-causal** scheme on top of the PID control.
- Why we can?
 - The cause of the ripple **is not external**.
 - Know the transition time beforehand.
 - Can delay the transition time.
 - Can calculate the compensation for the ripple.
- How to be risk free?
 - Make a **fast transition** in only 1 switching clock.
 - After transition, the normal PID will take over the control, adsorbing any PVT fluctuation.

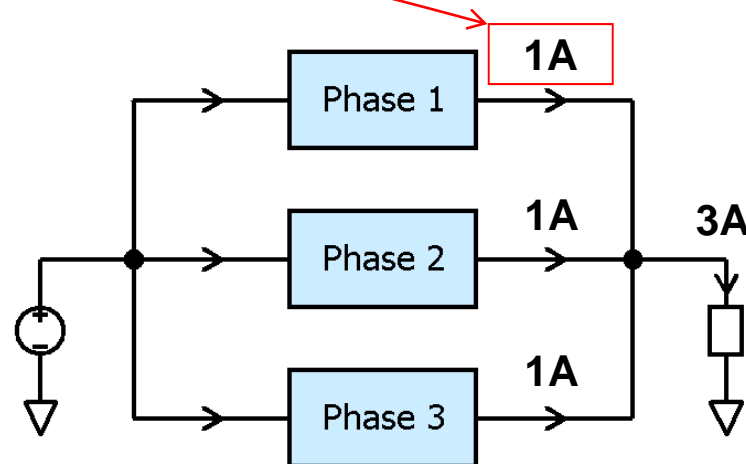
Strategy

Total current after transition = Total current before transition

minus 0.5A within 1 clock



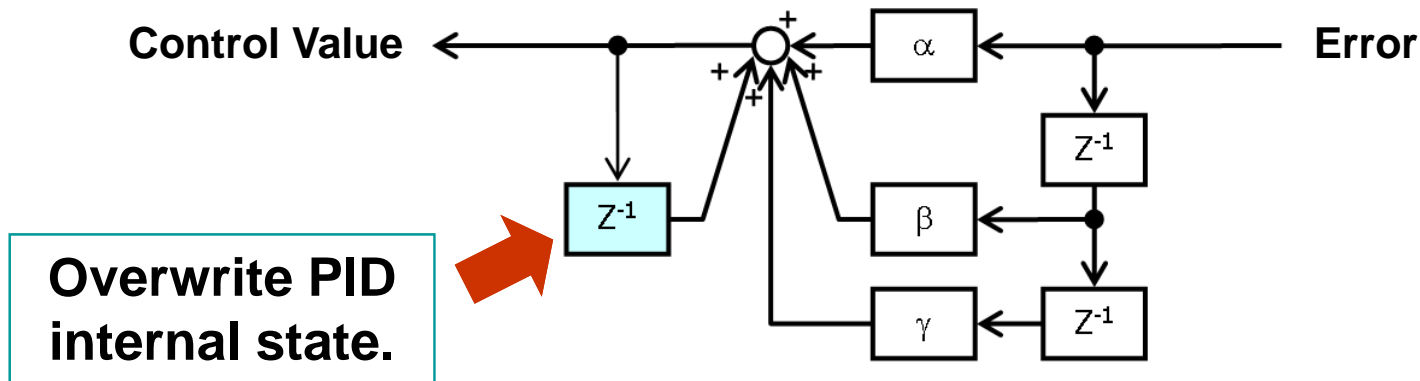
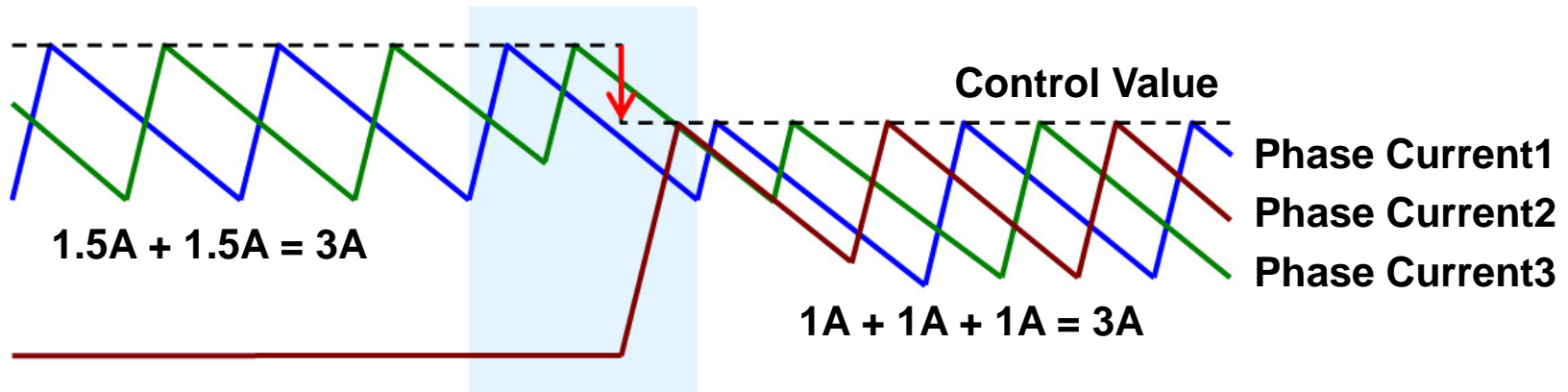
2-phase operation



3-phase operation

Control Value

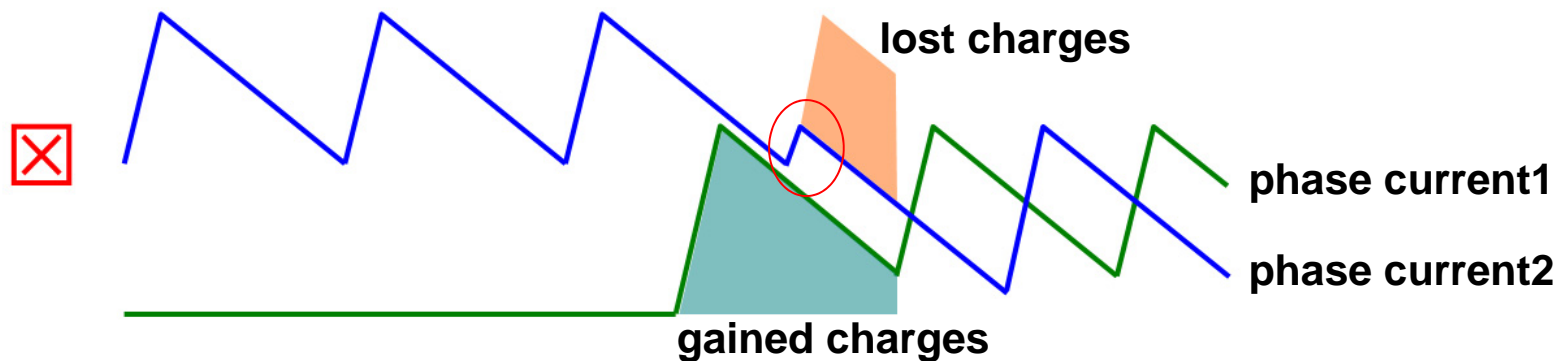
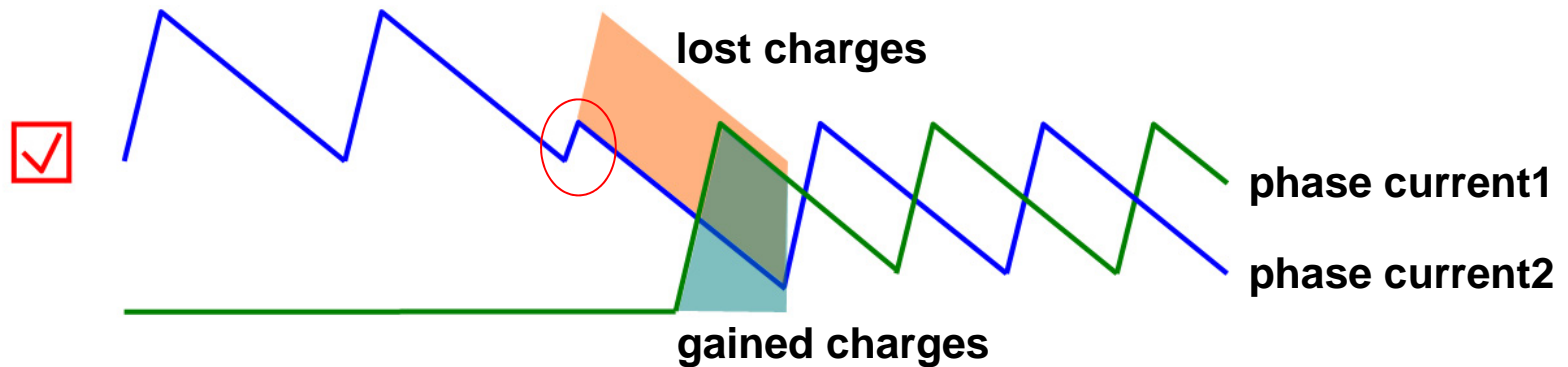
Shifting the control value.



Digital PID Compensator

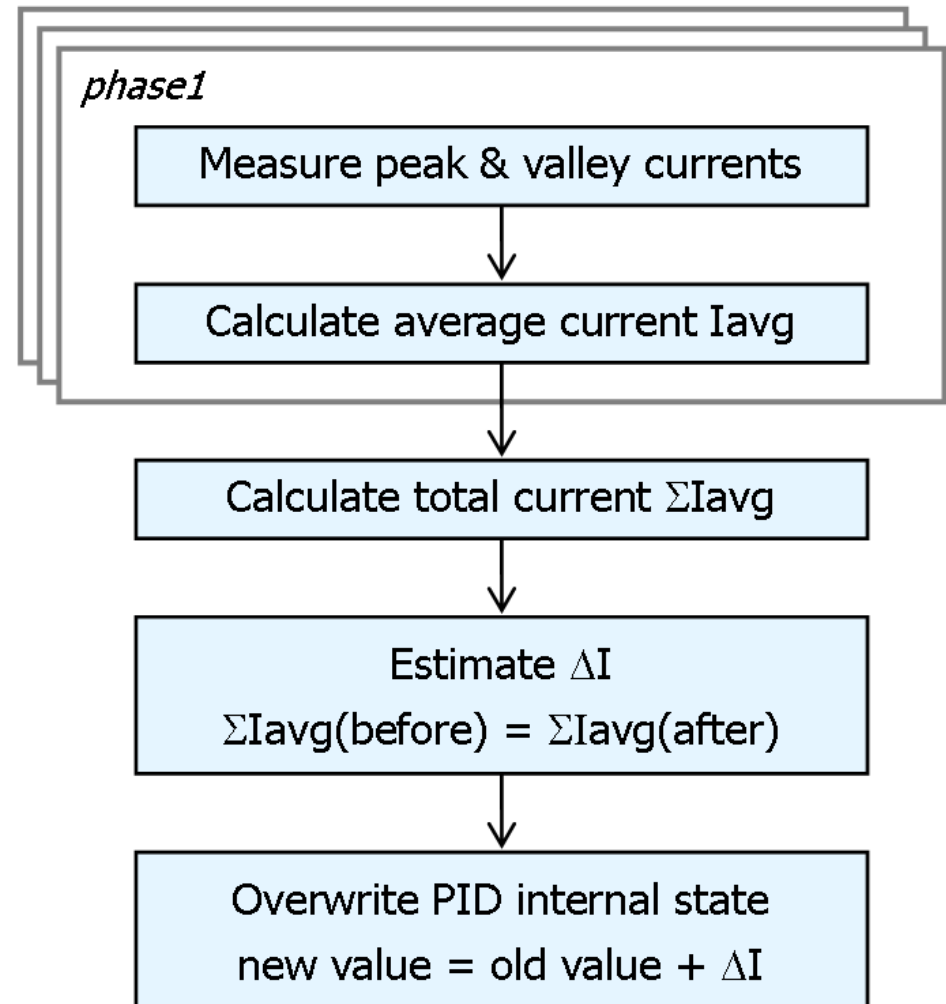
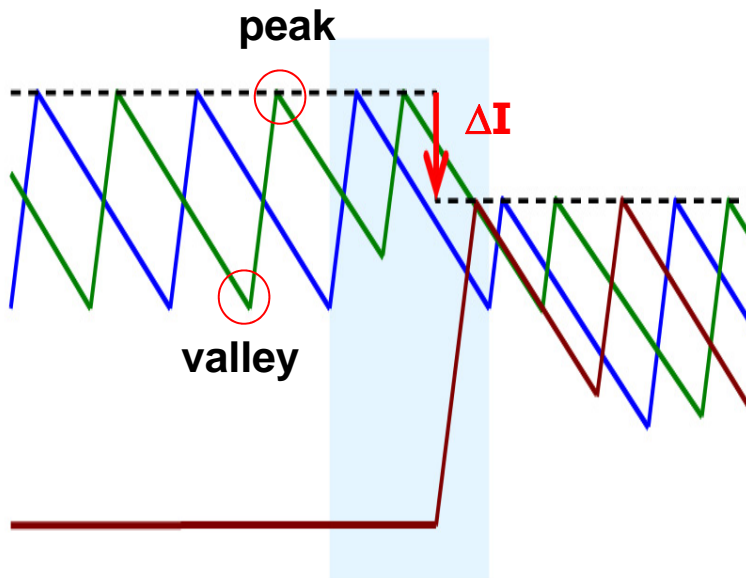
Sequence

Choose the sequence that minimizes the net change of charges.

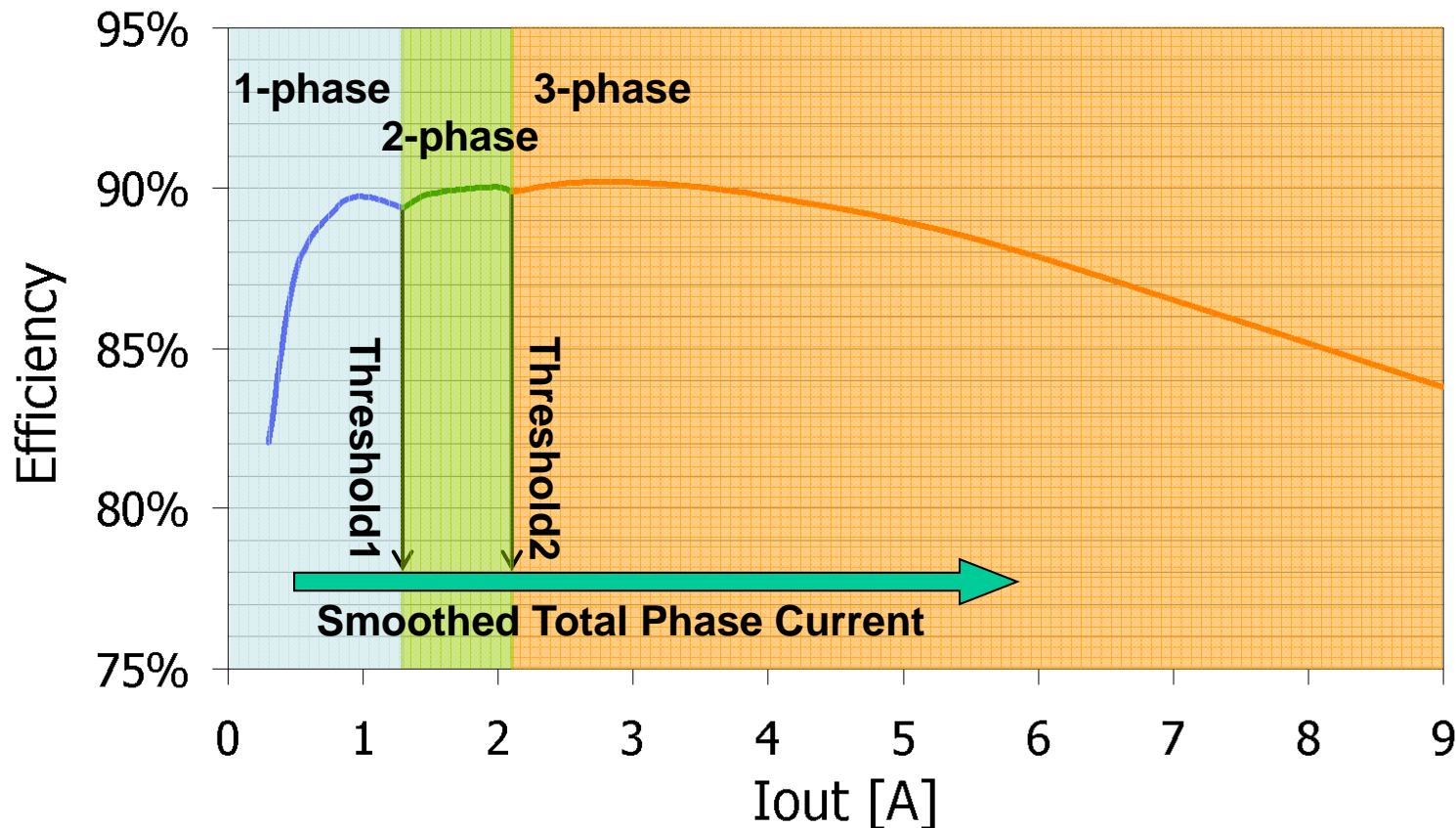


Calculations

Measure phase currents as digital values.

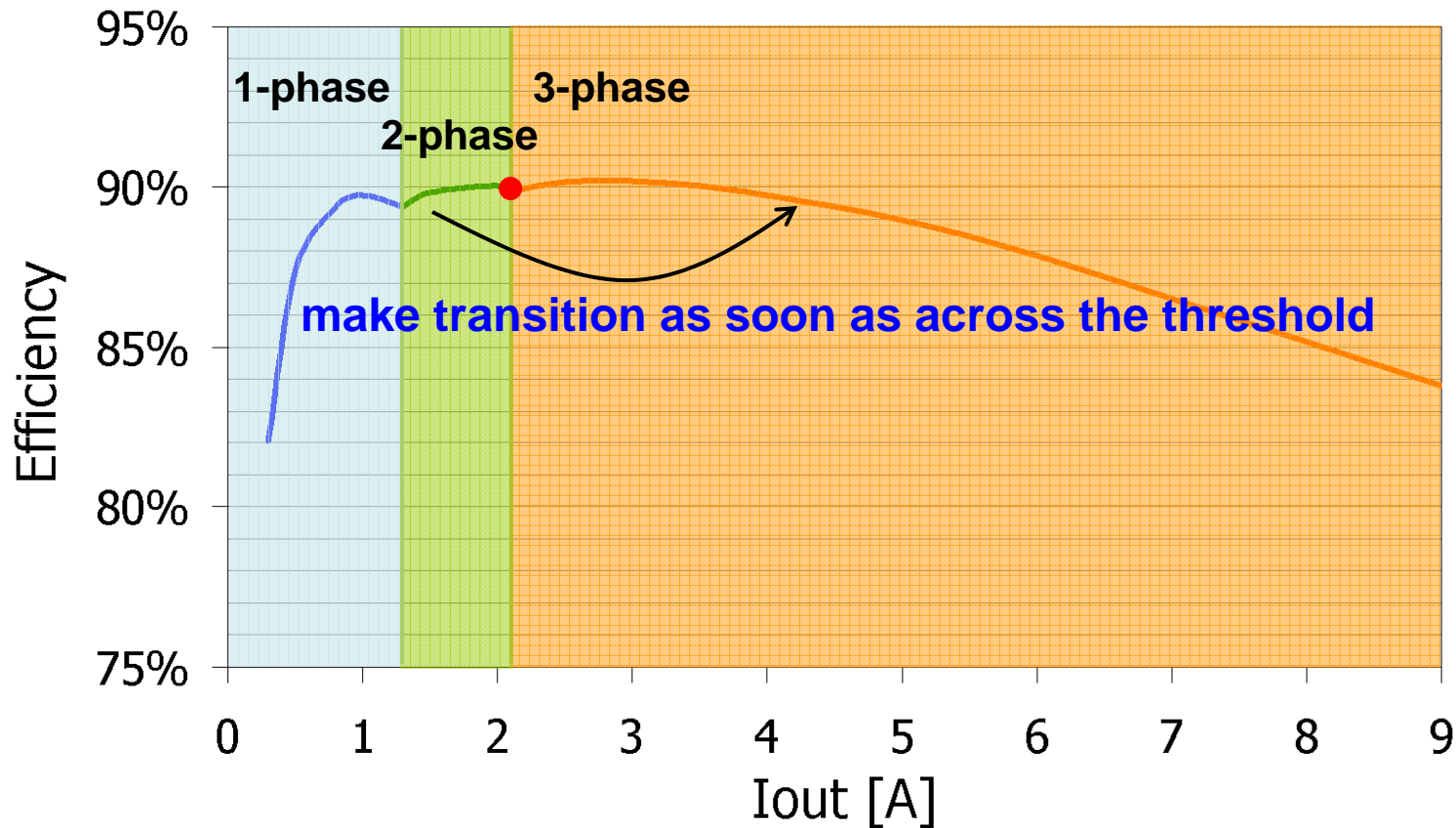


Transition Time



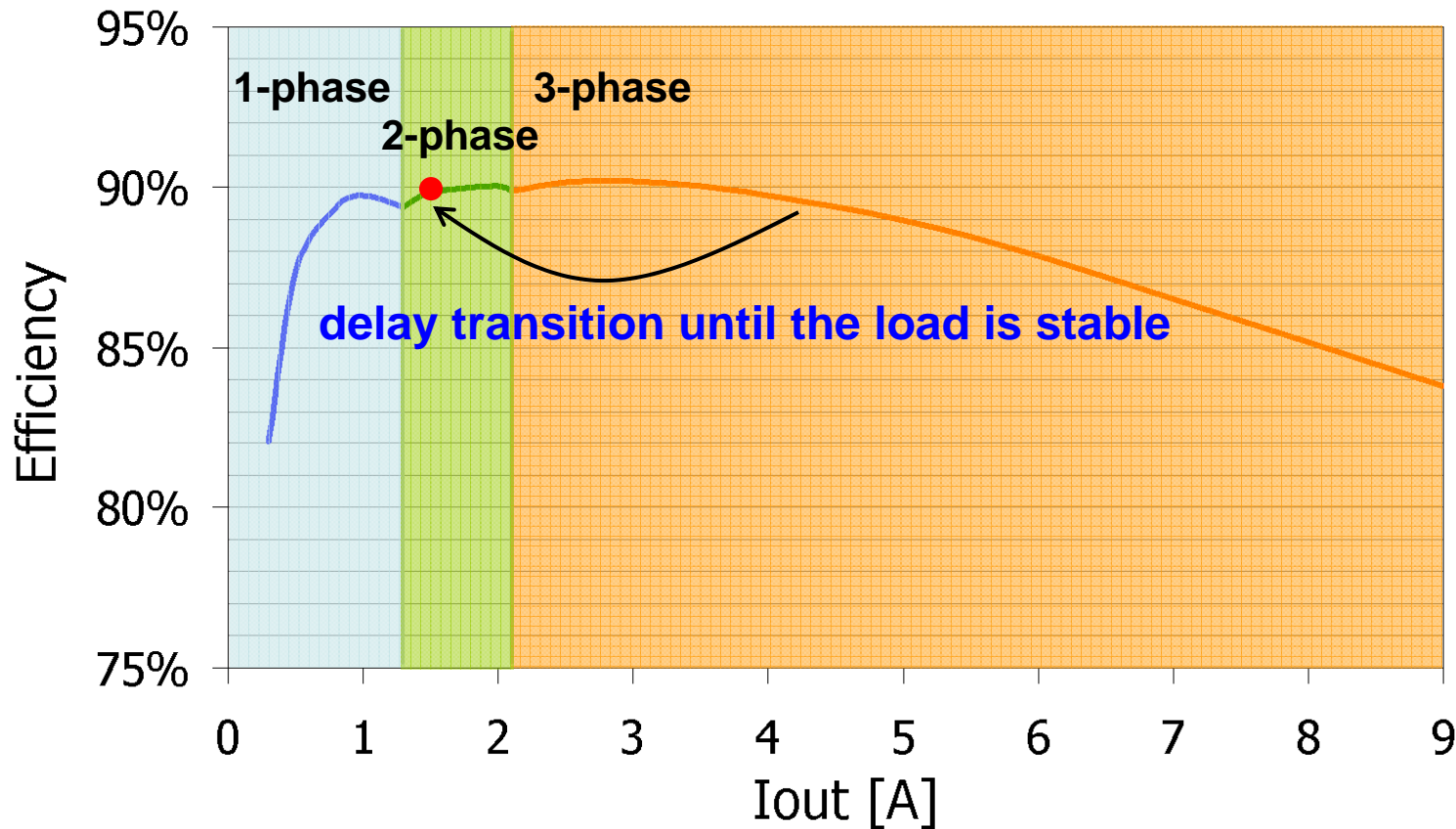
- Active phase count is determined by comparing smoothed total phase current with preset threshold values.
- Threshold values are predetermined by using the efficiency curves.
- Smoothed total phase current is calculated by using the control value times the active phase count.

Transition Time



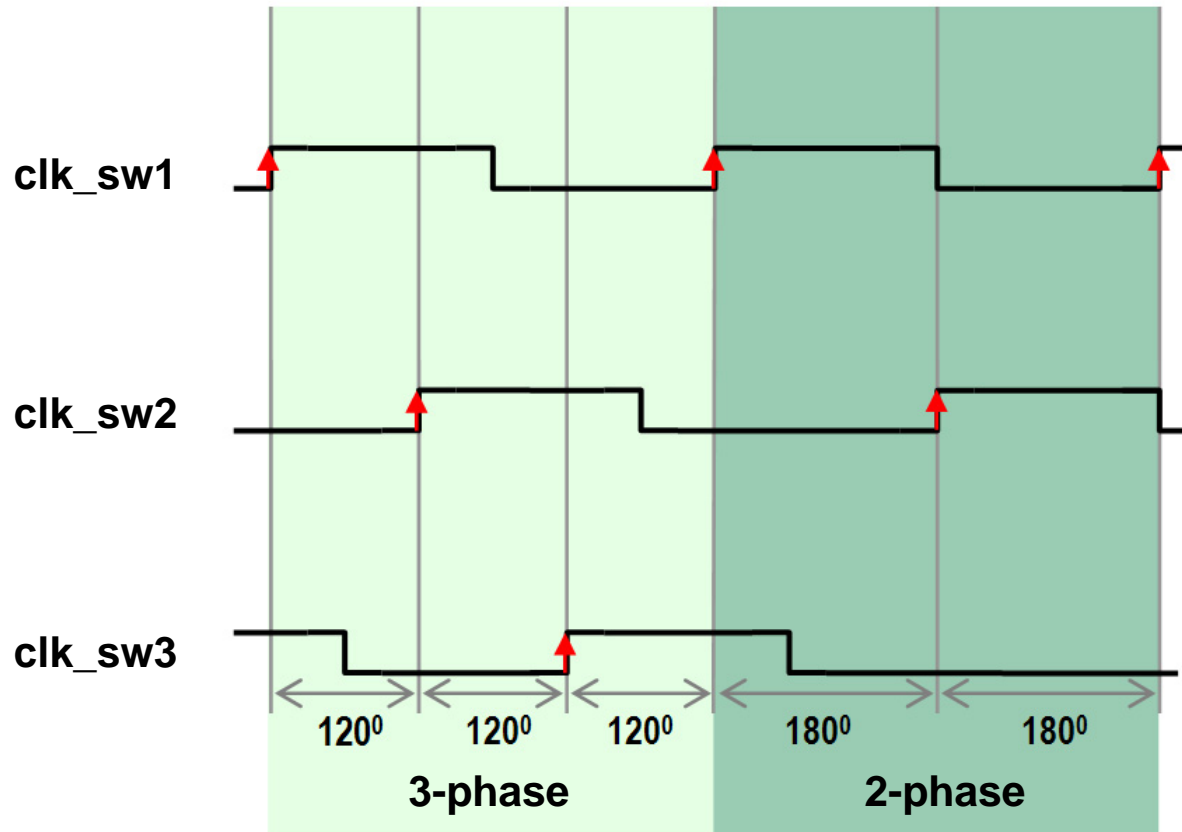
- For phase adding, make transition as soon as the total current across the threshold value.

Transition Time



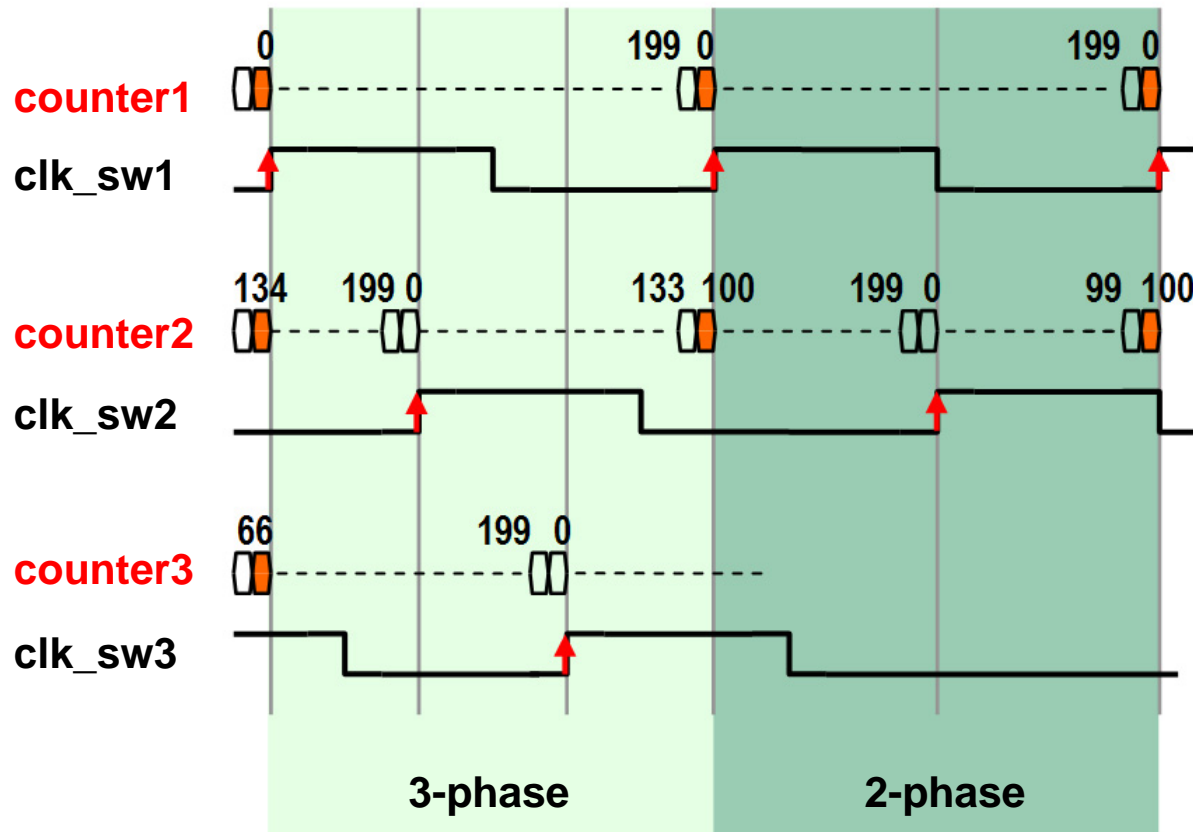
- For phase adding, make transition as soon as the total current across the threshold value.
- For phase dropping, delay transition until the load current is stable.

Switching Clock



- During transition, the phases of the switching clocks need to be reconfigured within 1 switching clock.

Switching Clock

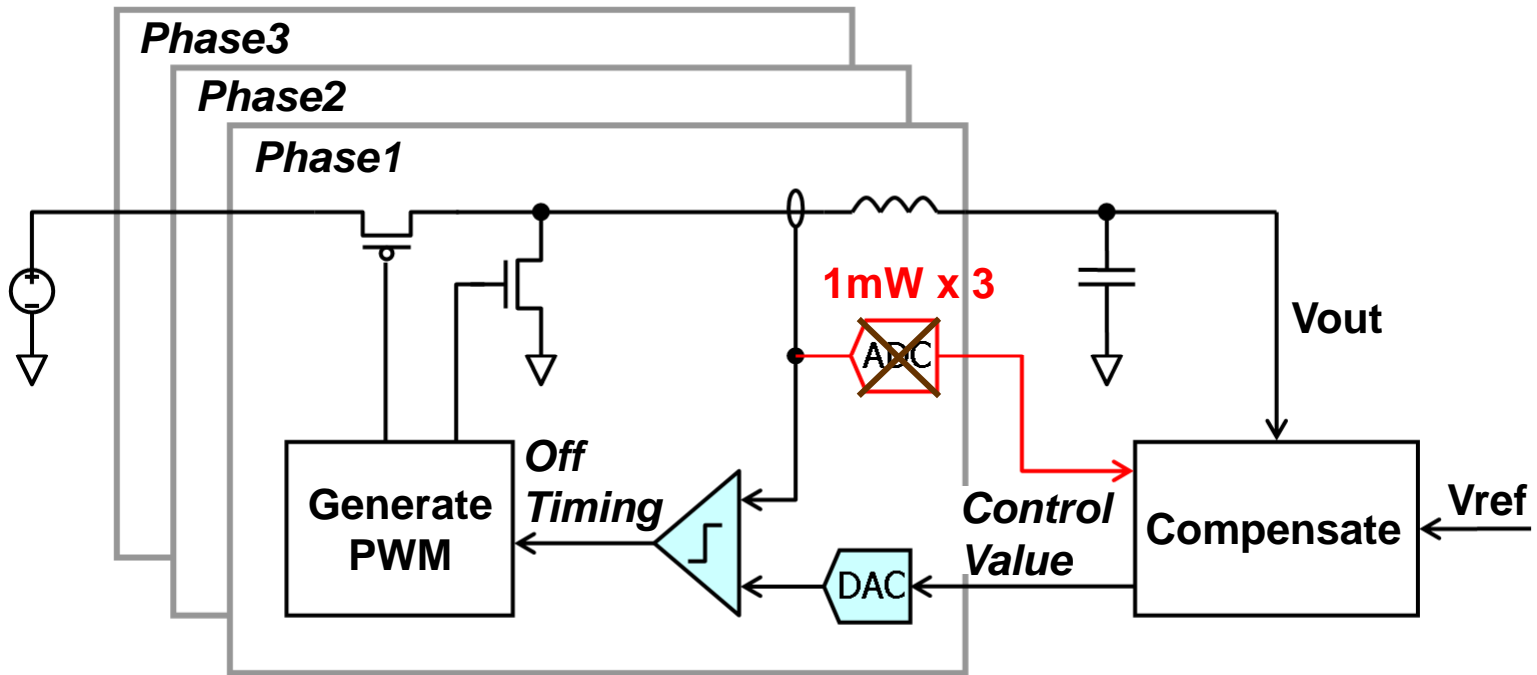


- Always synchronize contents of counter2 and counter3 when counter1=0.
- Phase balances are always maintained, and phase shifting can be completed in 1 switching clock.

Outline

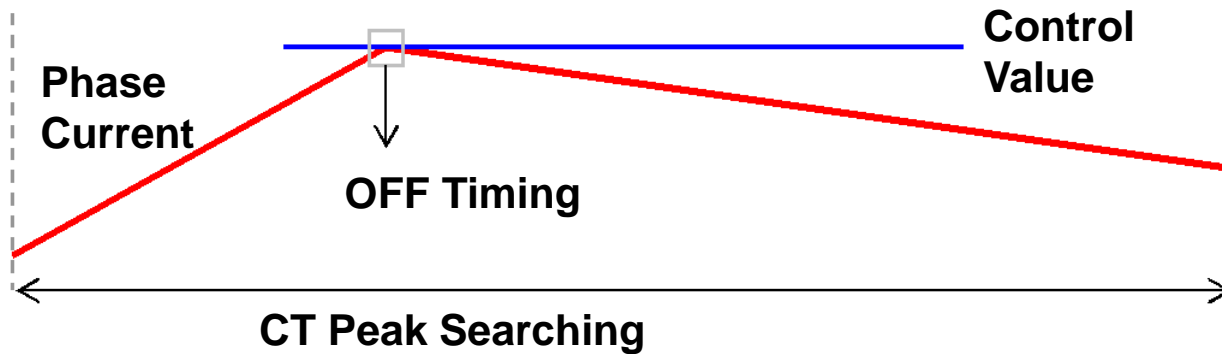
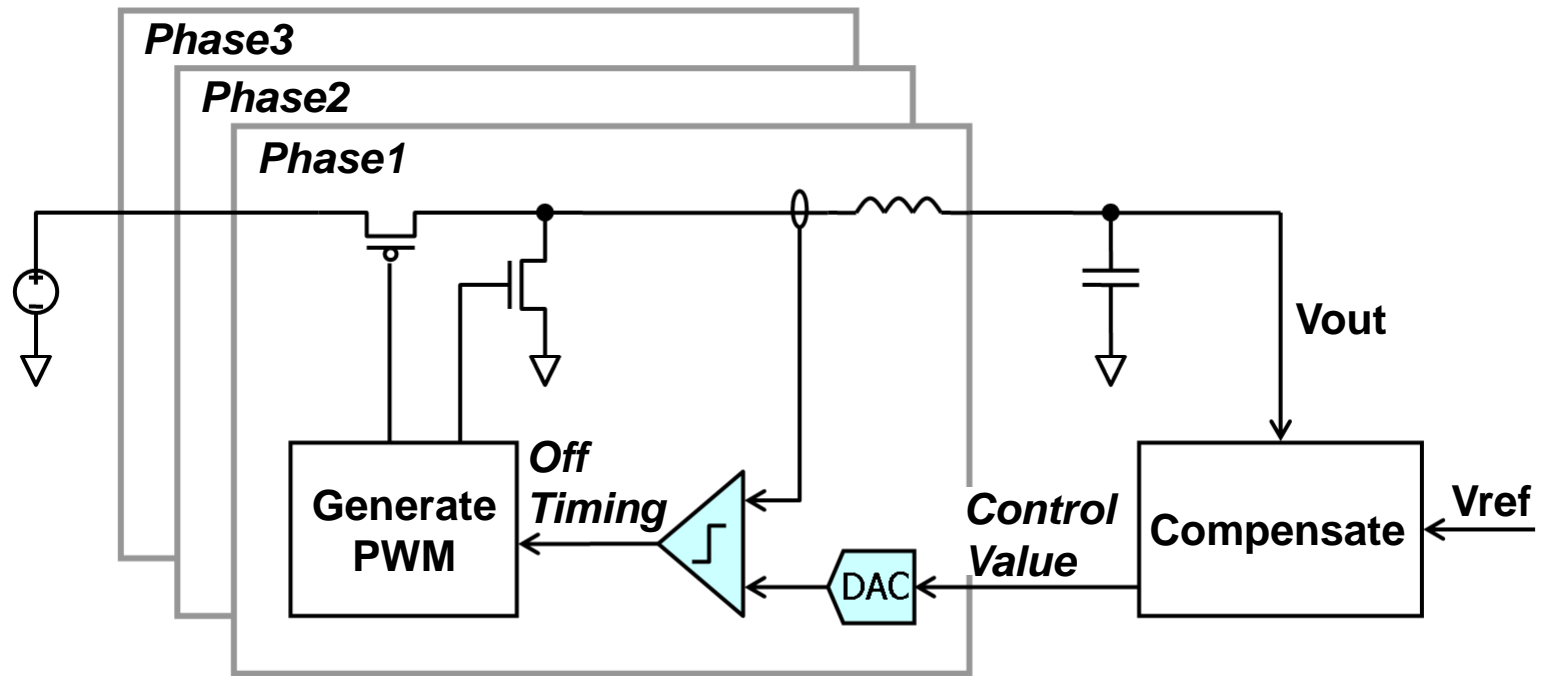
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Objective



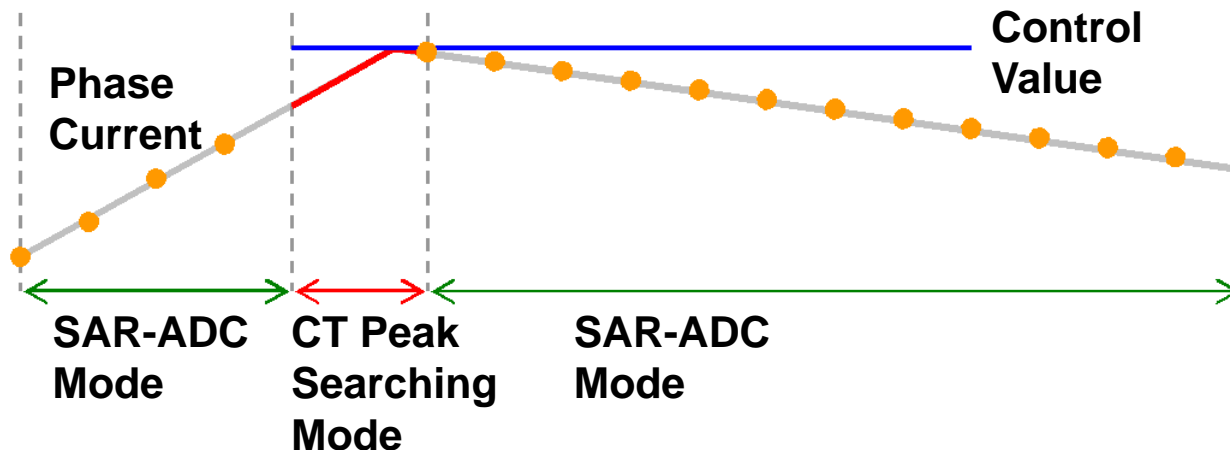
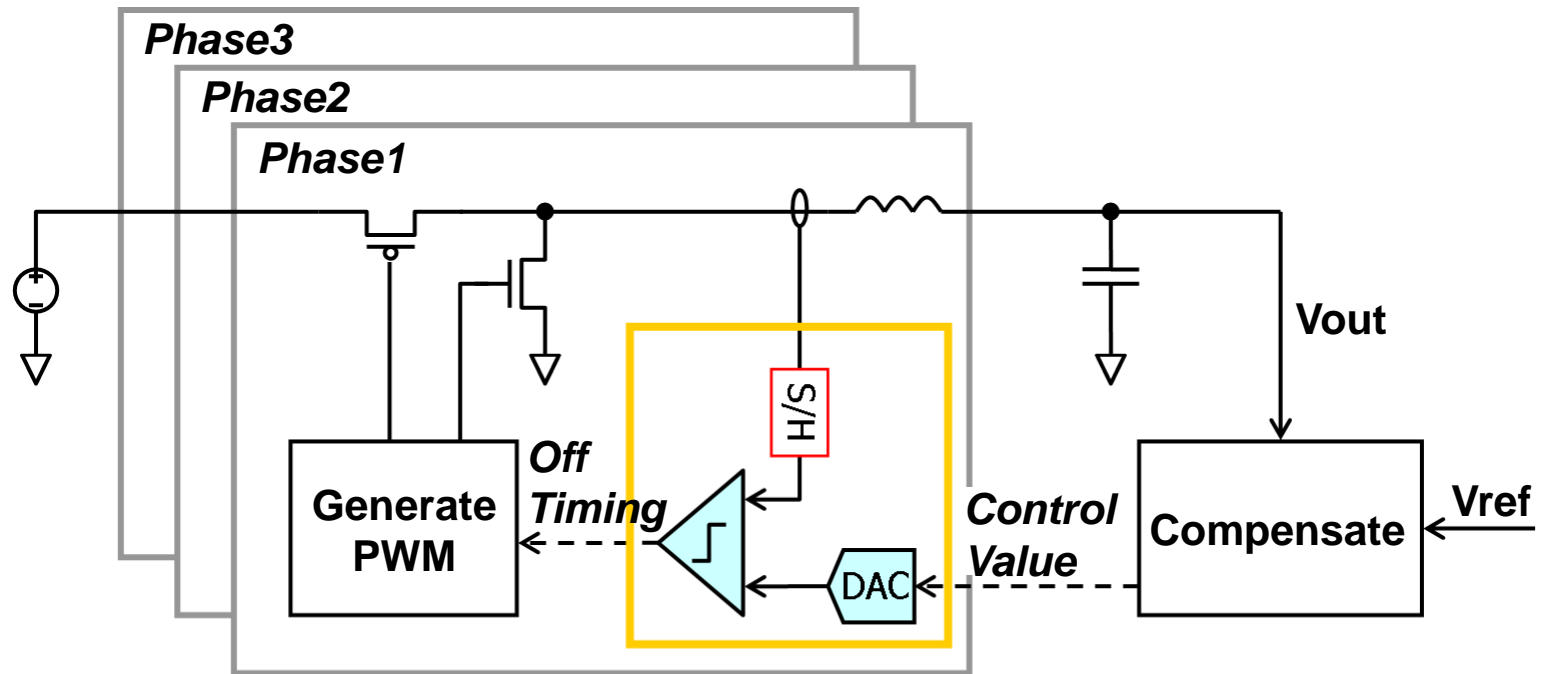
- ADCs consume 3mW, 28% of system power consumption.
- CT/DT hybrid current control is proposed to eliminate the 3mW, and improve the efficiency by 32% at 1mA load.
- The idea is to produce the digital data by time sharing of the existing comparator and DAC circuit.

Conventional Current Control



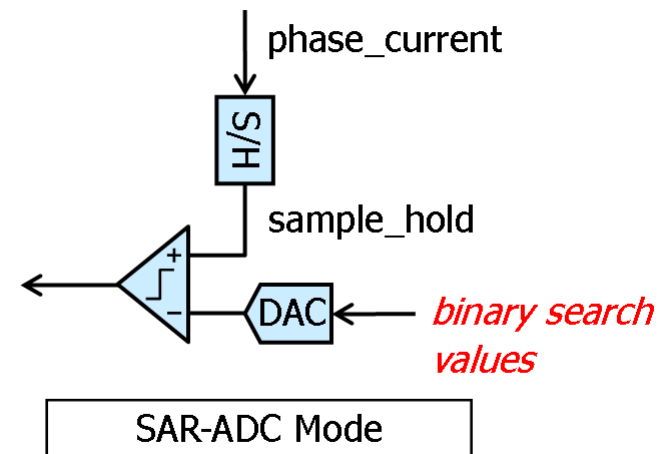
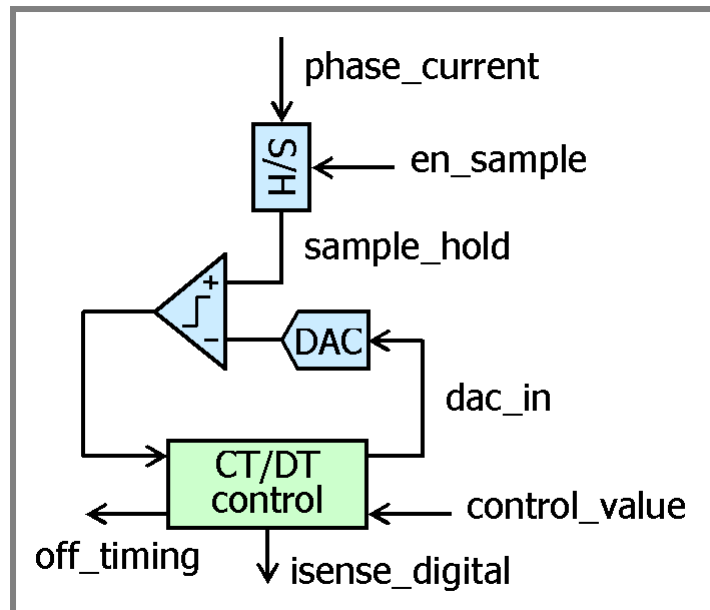
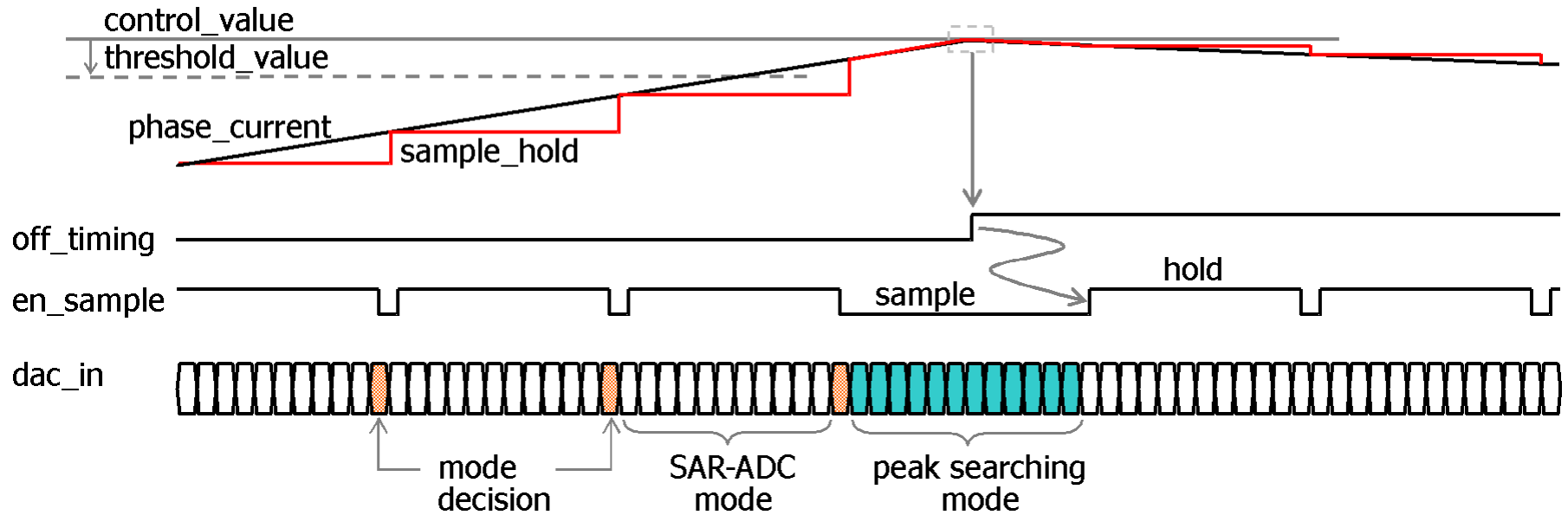
CT comparison is required to avoid a limit cycle.

New Hybrid Current Control

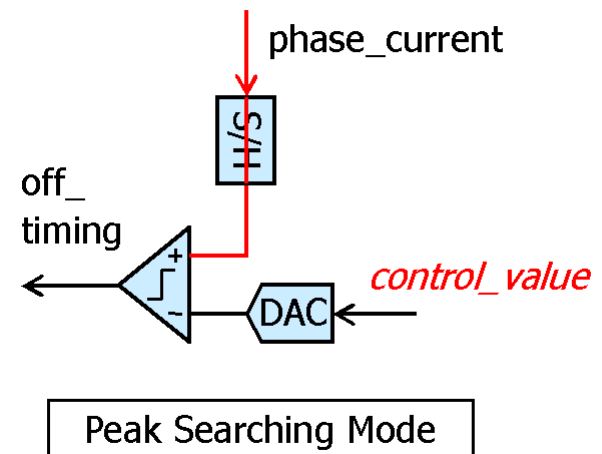
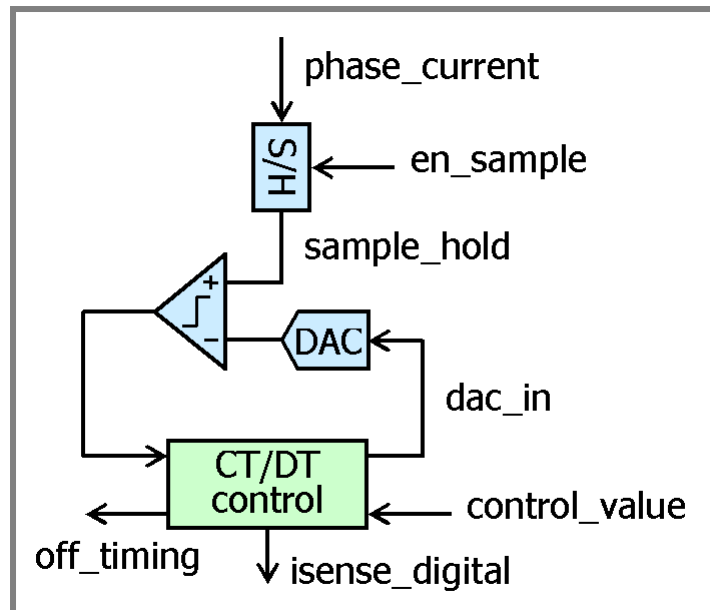
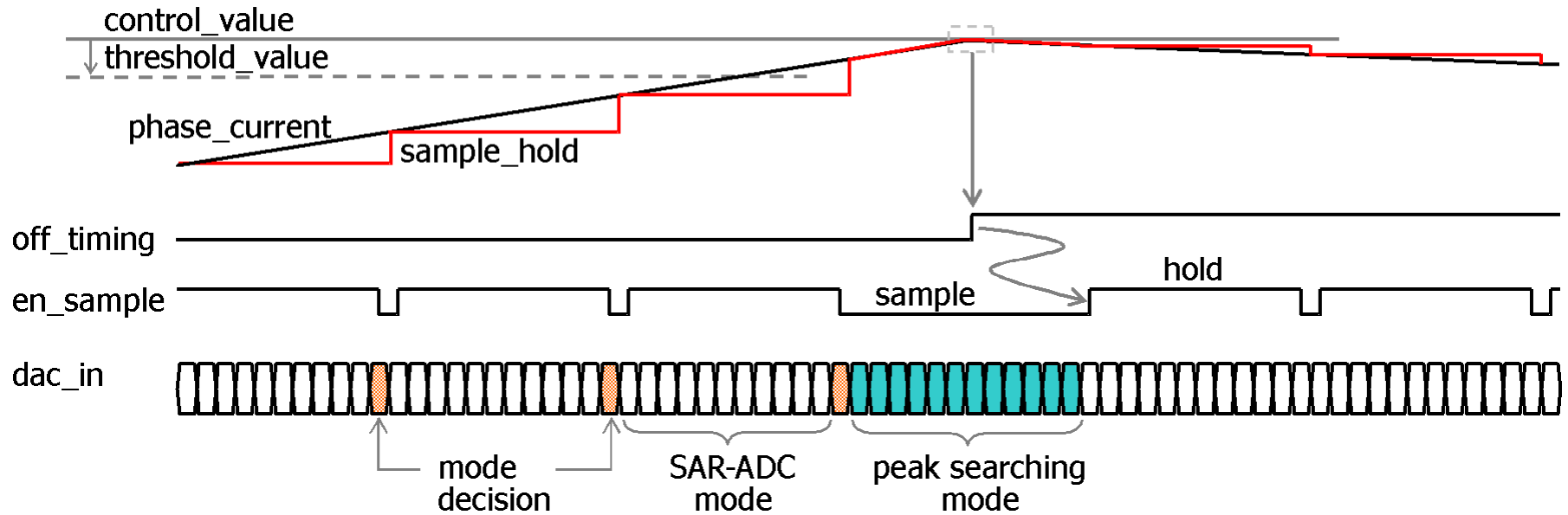


Produce CT resolution of the OFF timing, while producing 11-bit 8MS/s data.

Timing



Timing

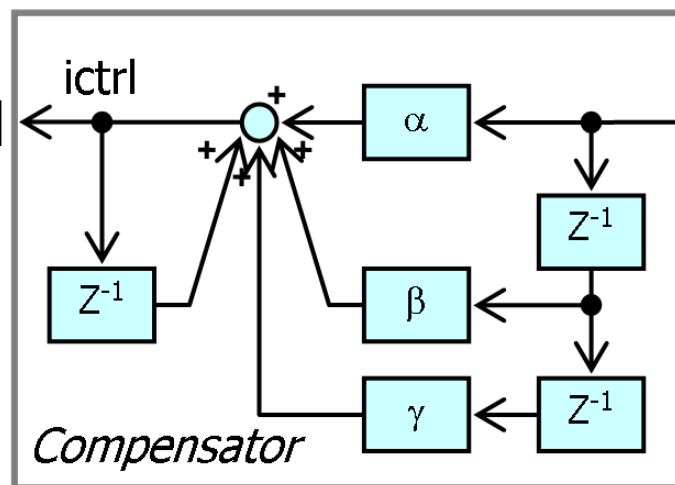
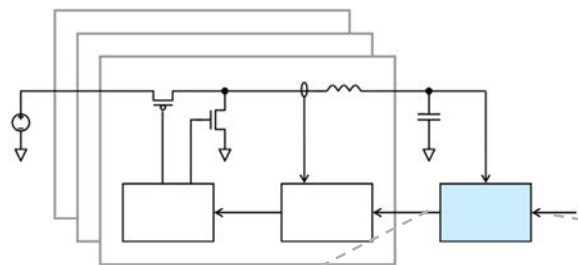


Outline

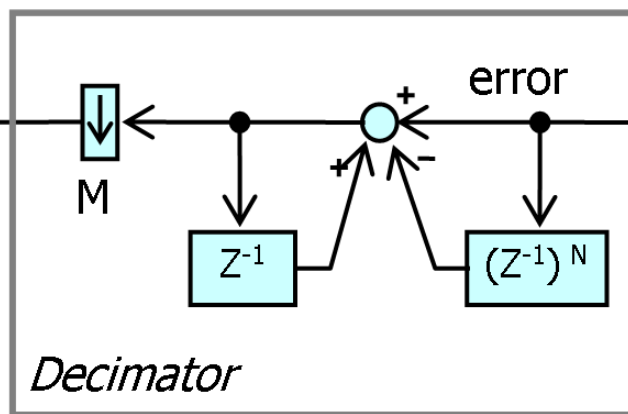
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Enhanced Voltage Feedback

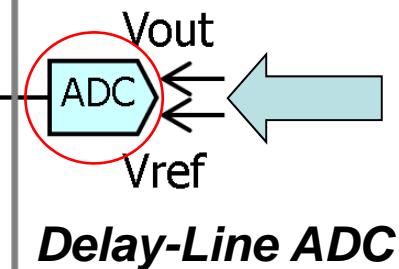
Raise SNR of the Vout feedback and lower the loop delay.



PID control
1.5MHz



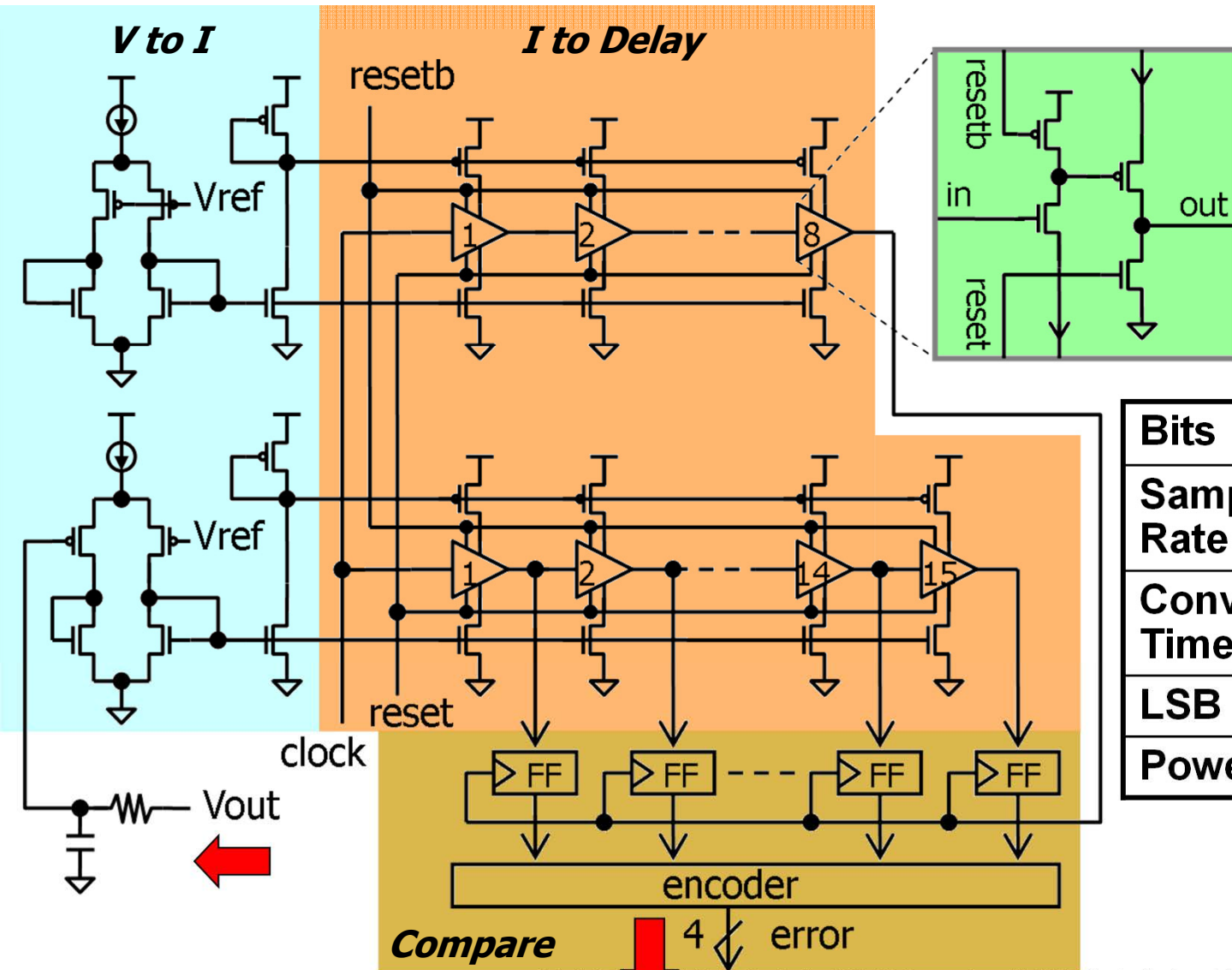
Smoothing
20MHz



Oversampling
4-bit 20MS/s

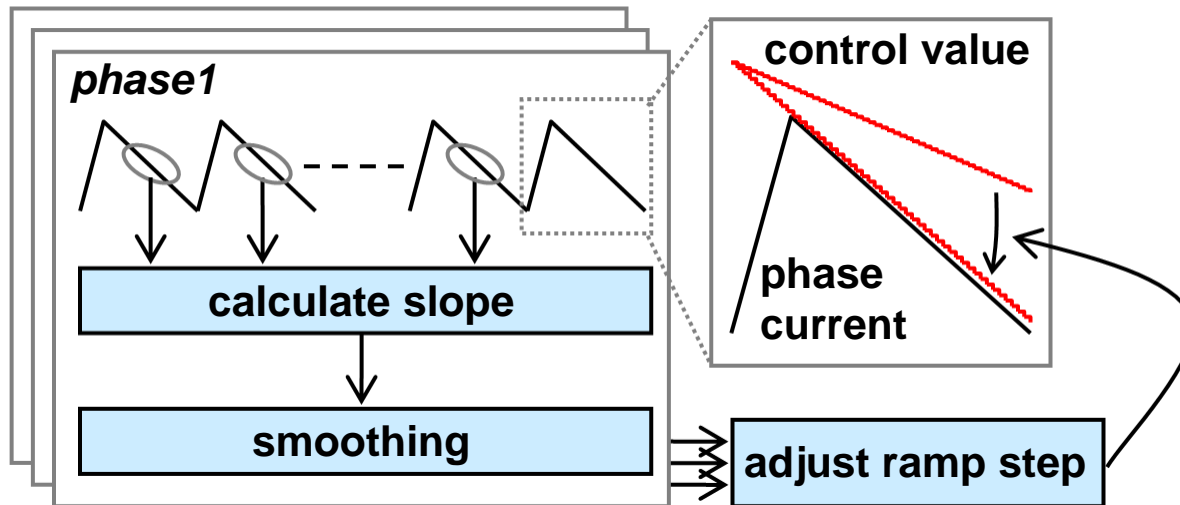
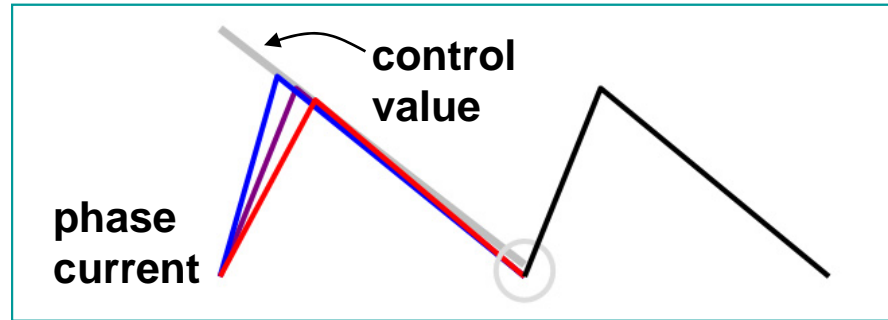
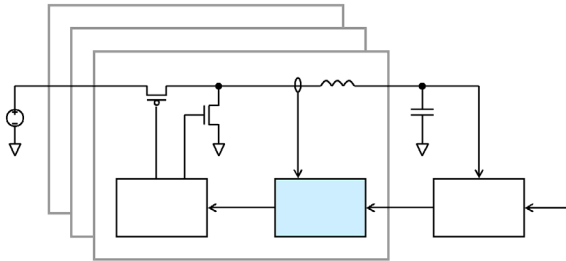
Delay-Line ADC

Design a high-speed, low-latency and low-power ADC.



Bits	4 bits
Sampling Rate	20MS/s
Conversion Time	50ns
LSB	5mV
Power	20 μ A/MHz

Adaptive Ramp

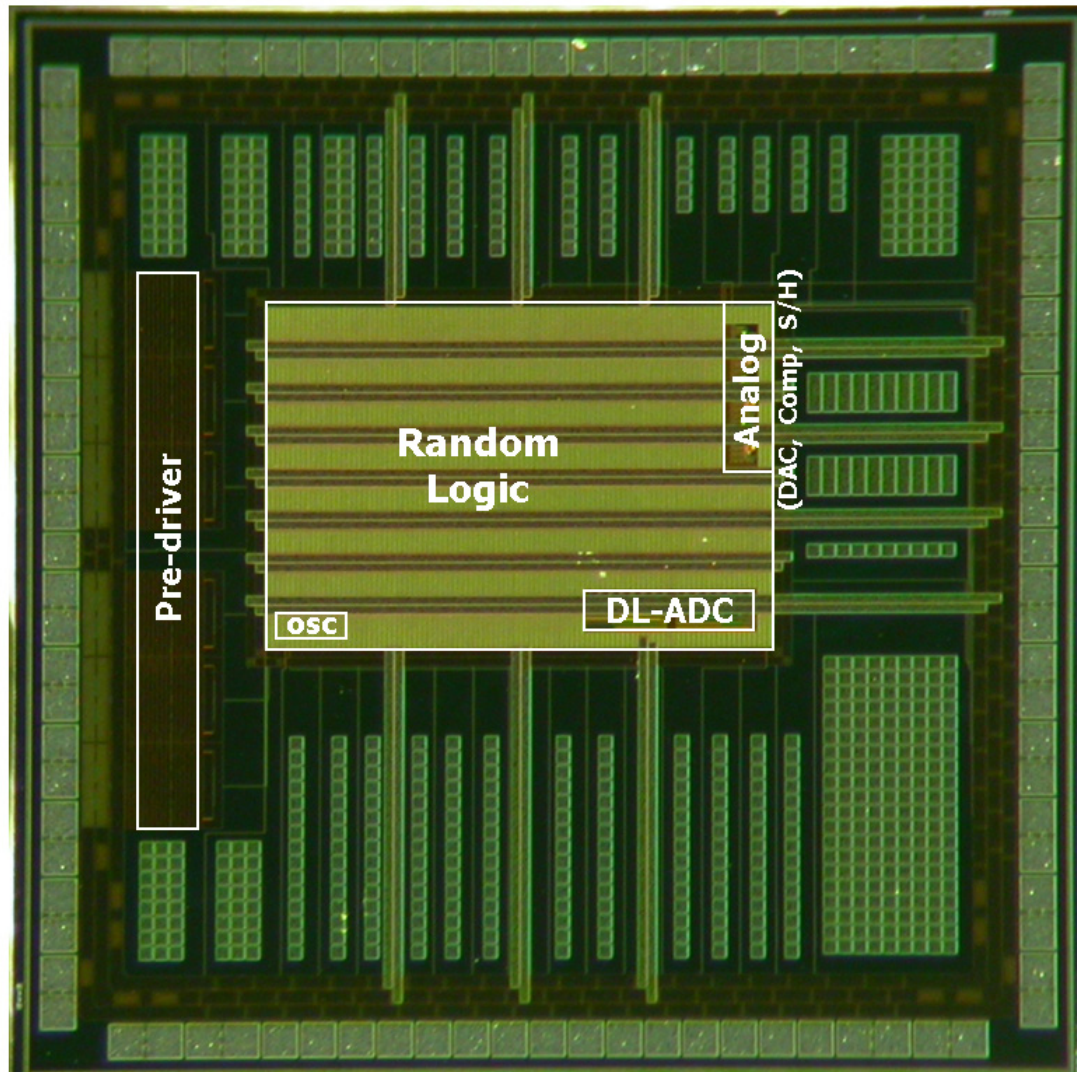


- Slope compensation needs to be added to the control signal, to stabilize the system from the influence of the current noise.
- The slope is adaptively tuned to be close to the falling slope of the phase current.

Outline

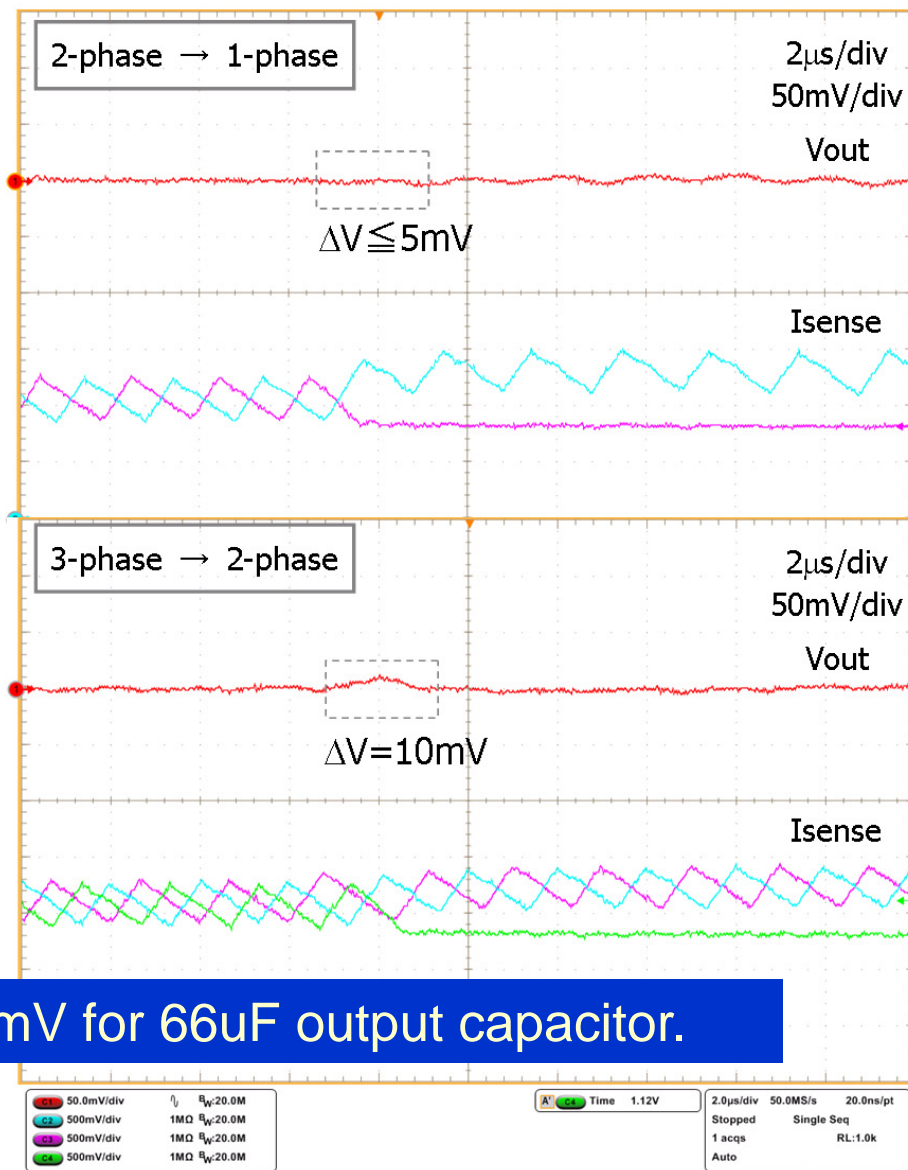
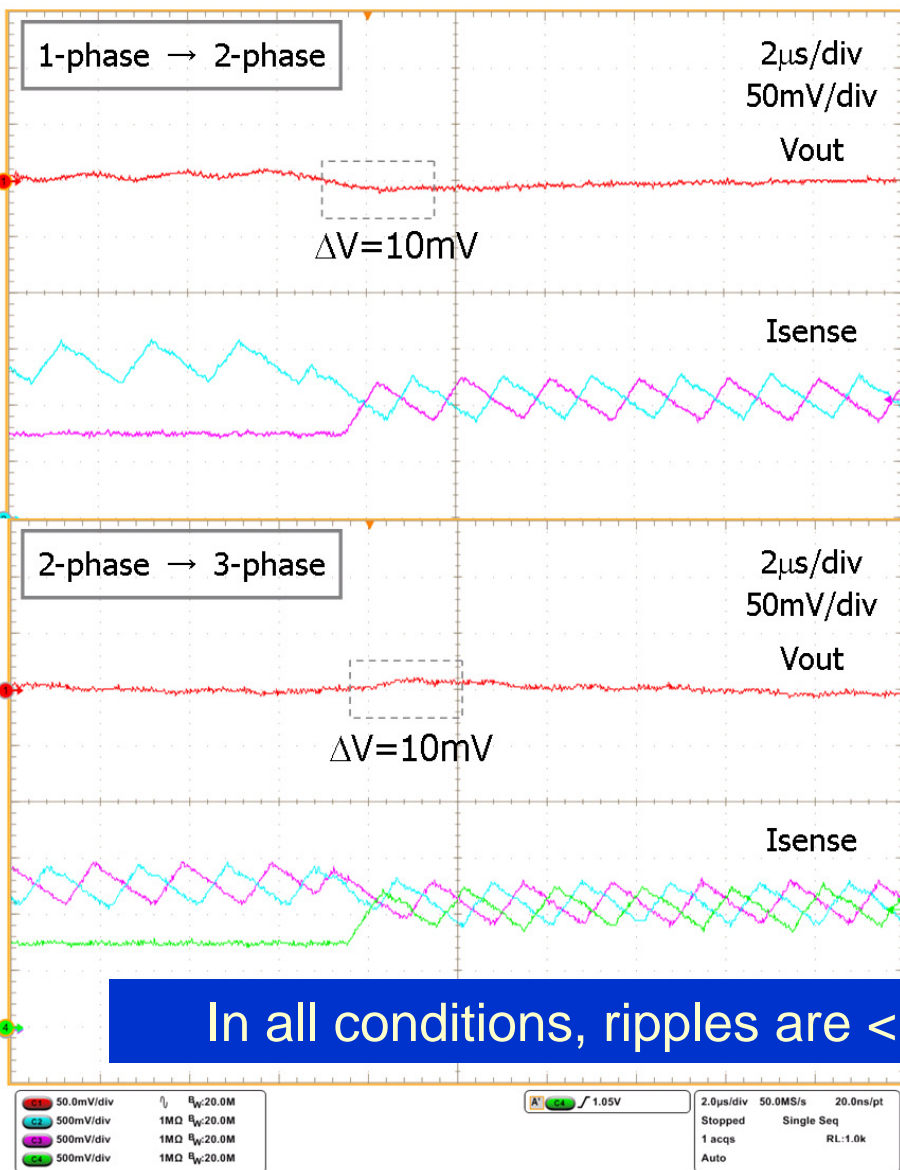
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Chip Micrograph



Features	
Technology	0.25 μ m 2.5V/5V CMOS
Phase Count	3
Max. Iout	9A
Fsw	500kHz
Core Frequency	100MHz
Vin	2.8V to 5.5V
Vout	0.2V to 3.3V
L (DCR)	2.2 μ H (13m Ω)
C	66 μ F
Logic Gate Count	24k gates
Chip Size	2.5mm x 2.5mm

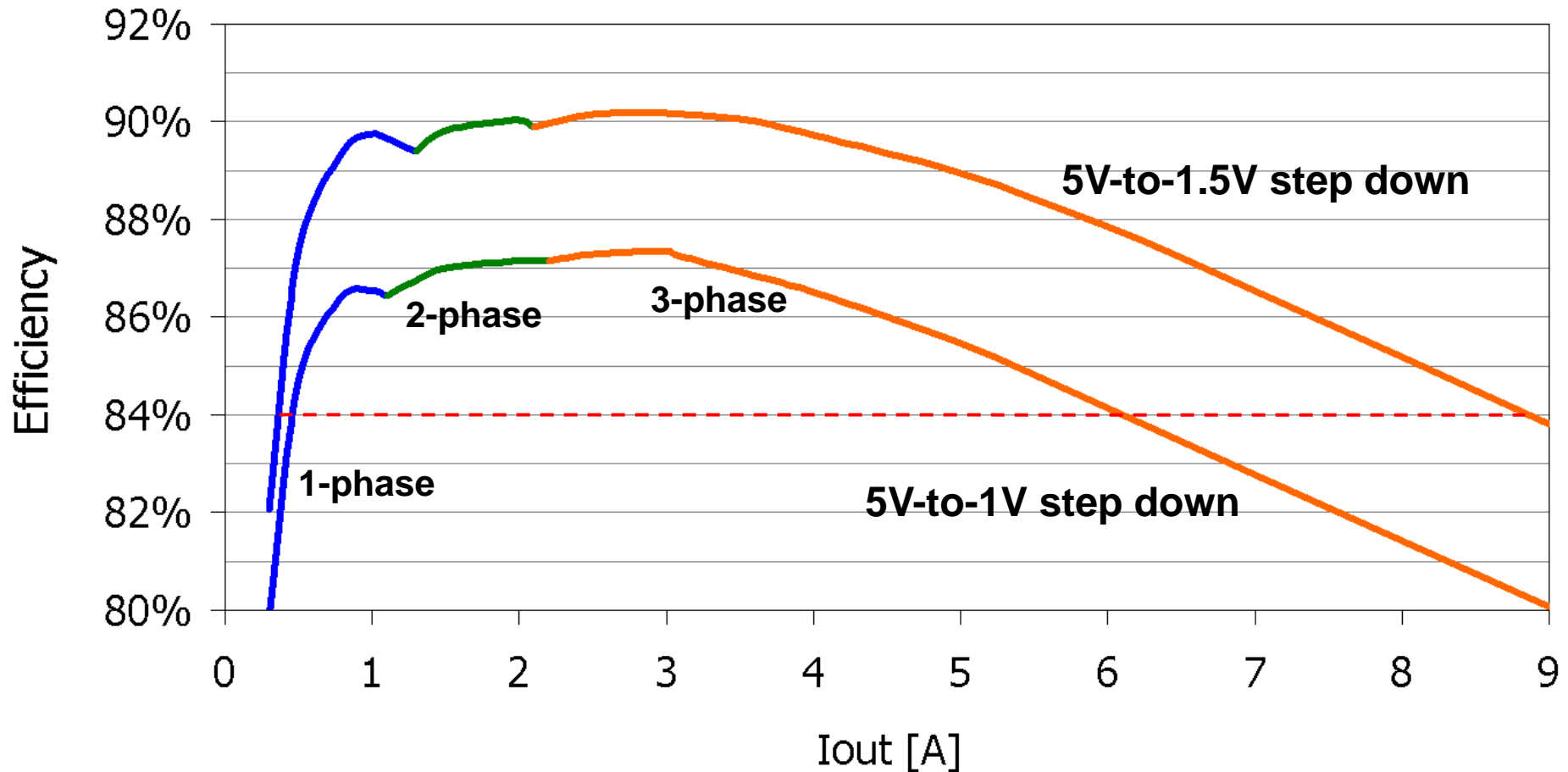
Measured Transient Ripples



In all conditions, ripples are <10mV for 66 μ F output capacitor.

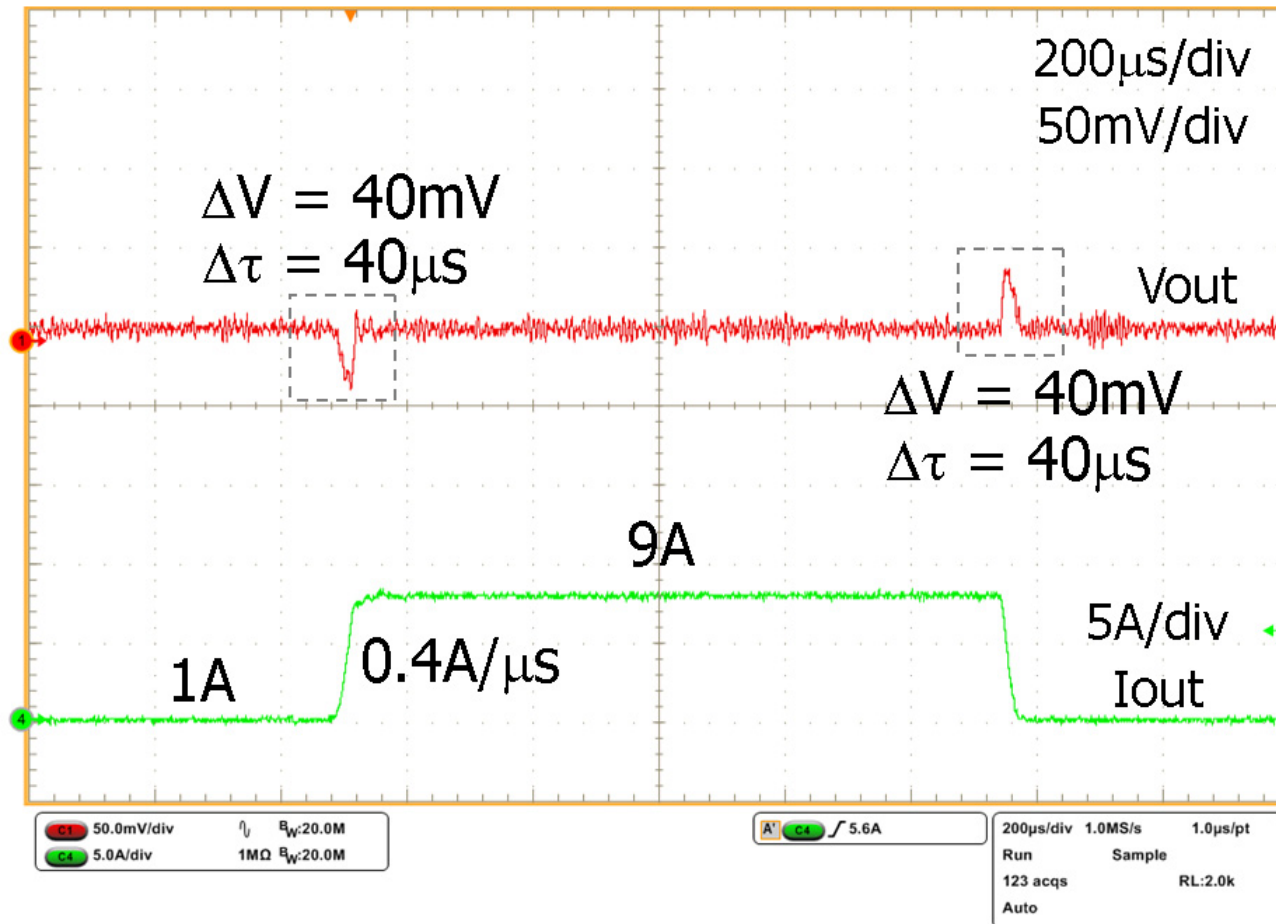
* $f_{sw} = 500\text{kHz}$, $C_{out} = 66\mu\text{F}$, $L = 2.2\mu\text{H}$

Measured Efficiency



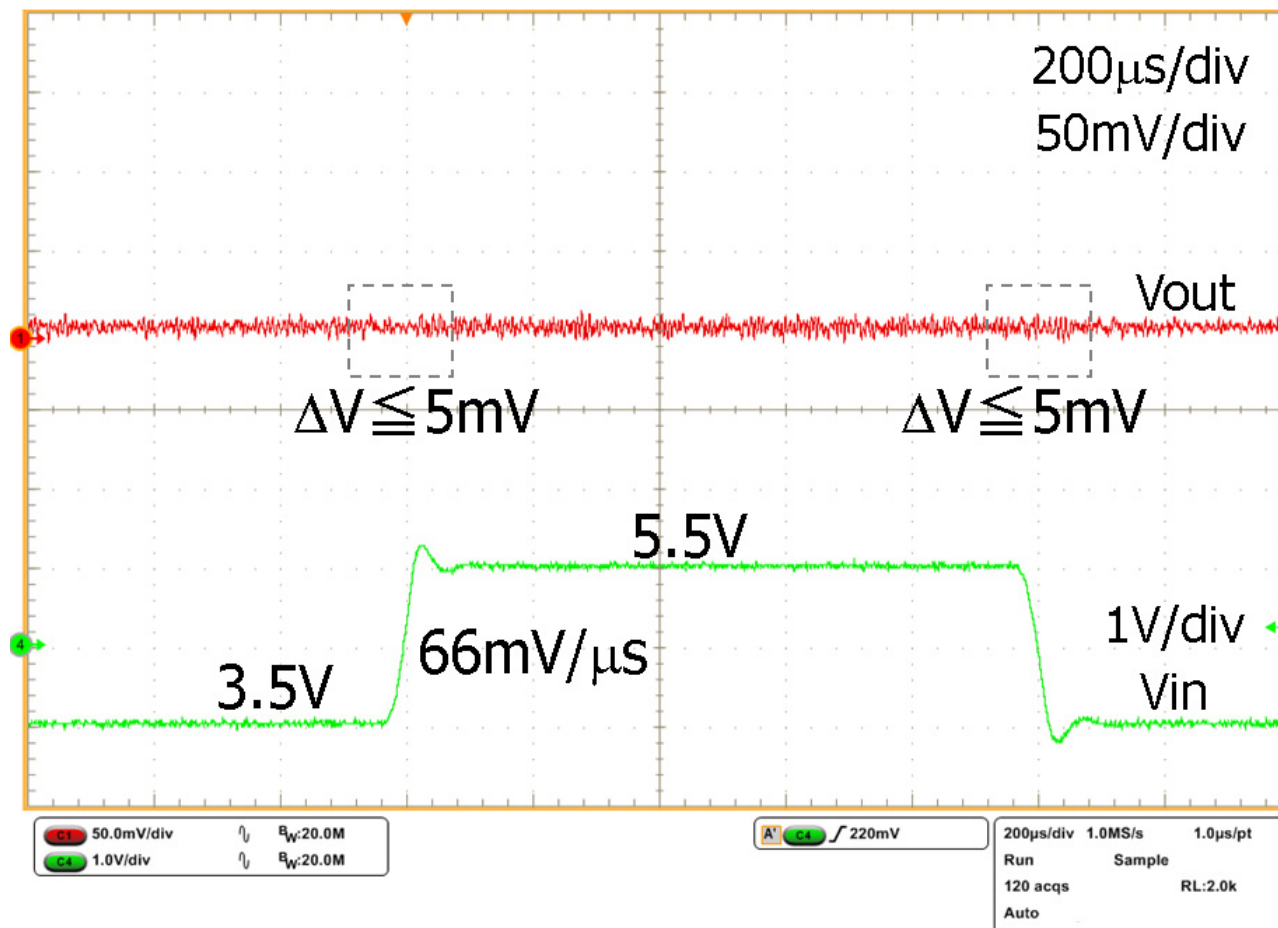
* $f_{sw} = 500kHz$, $C_{out} = 66\mu F$, $L = 2.2\mu H$

Measured Load Transient Response



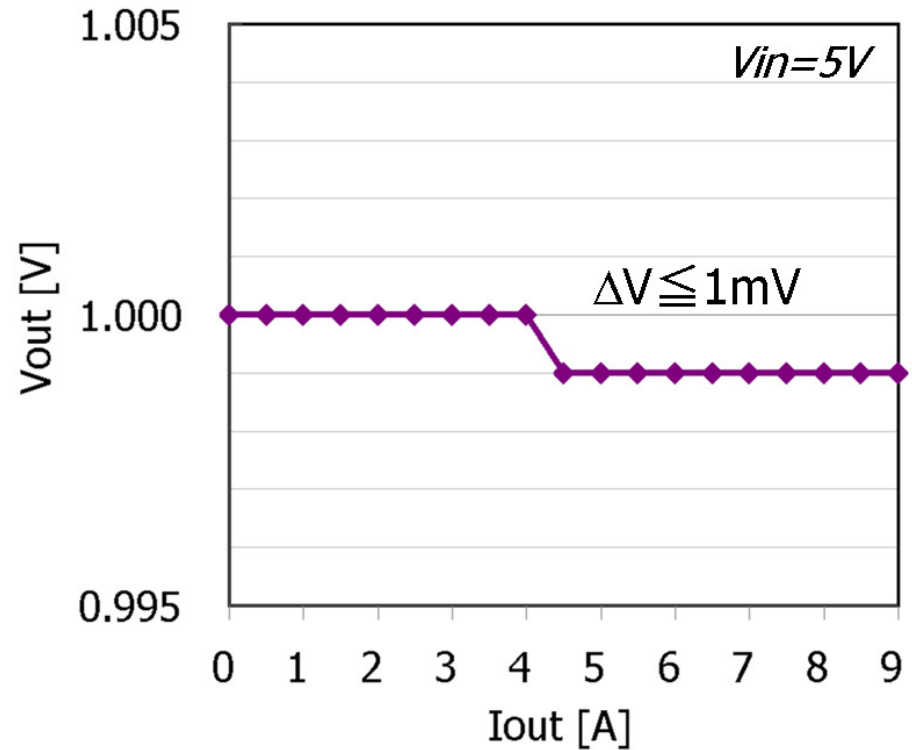
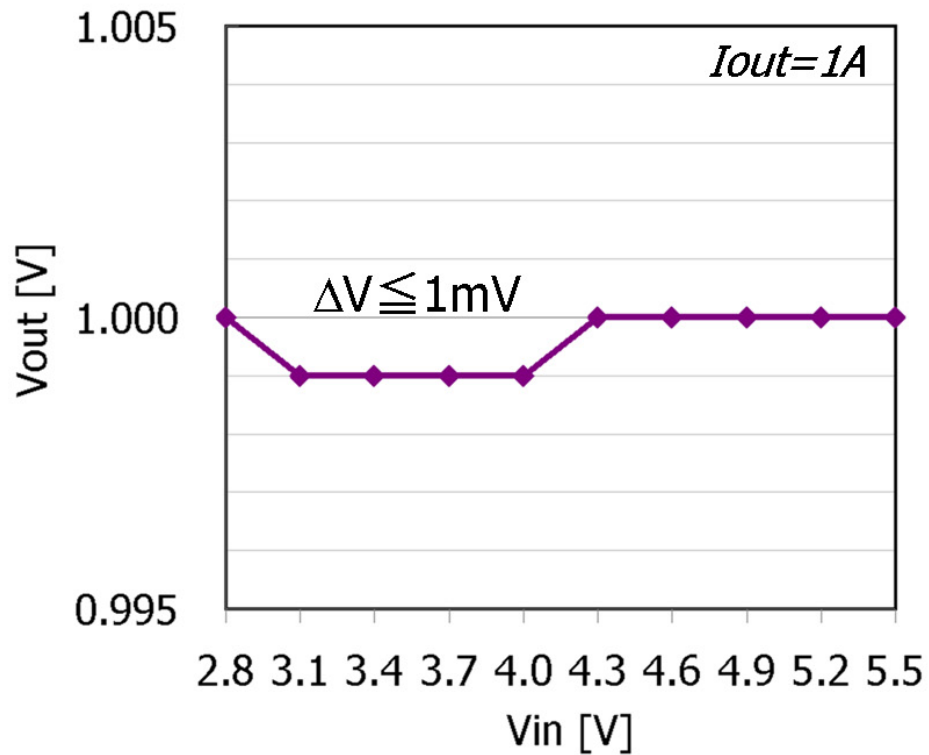
* $f_{sw} = 500\text{kHz}$, $C_{out} = 66\mu\text{F}$, $L = 2.2\mu\text{H}$

Measured Line Transient Response



* $f_{sw} = 500\text{kHz}$, $C_{out} = 66\mu\text{F}$, $L = 2.2\mu\text{H}$

Measured Line/Load Regulation



Comparison

	ASSCC2005	ISSCC2013	This Work
Technology	0.35 μ m CMOS	0.13 μ m CMOS	0.25 μ m CMOS
Phase Count	2	4	3
Control Architecture	Digital	Analog	Digital
F _{sw}	313kHz	100MHz	500kHz
V _{in}	3.3V	1.2V	2.8V~5.5V
V _{out}	1.5V	0.6V~1.05V	0.2V~3.3V
Max. I _{out}	15A	1.2A	9A
L	2 μ H	8nH	2.2 μ H
C	2000 μ F	3.05nF	66 μ F
Peak Efficiency (η)	80%@3.3V→1.5V	82.4%@1.2V→0.9V	90.2%@5V→1.5V
Good Load Range	-	0.1A~0.8A @ η >80%	0.4A~9A @ η >84%
Load Response	80mV@8A step	60mV@0.18A step, 0.2A/ μ s	40mV@8A step, 0.4A/ μ s
Line Response	-	-	5mV@2V step, 66mV/ μ s
Line/Load Regulation	-	-	1mV

Summary

- A 3-phase DC-DC converter is presented.
 - 84%-to-90% efficiency over 0.4A-to-9A load.
- Phase adding/dropping scheme :
 - 1-cycle fast transition.
 - <10mV ripple with only 66 μ F output capacitors.
- CT/DT hybrid current control :
 - 28% power saving of the system power consumption.
 - offering a CT resolution of the PWM duty, while producing 11bit digital data.
- Fast response configuration :
 - <40mV fluctuation during an 8A load transition.
 - <5mV fluctuation during a 2V line transition.

The End

A 6A 40MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient

Min Kyu Song, Joseph Sankman, and Dongsheng Ma

Integrated System Design Laboratory
Texas Analog Center of Excellence
The University of Texas at Dallas



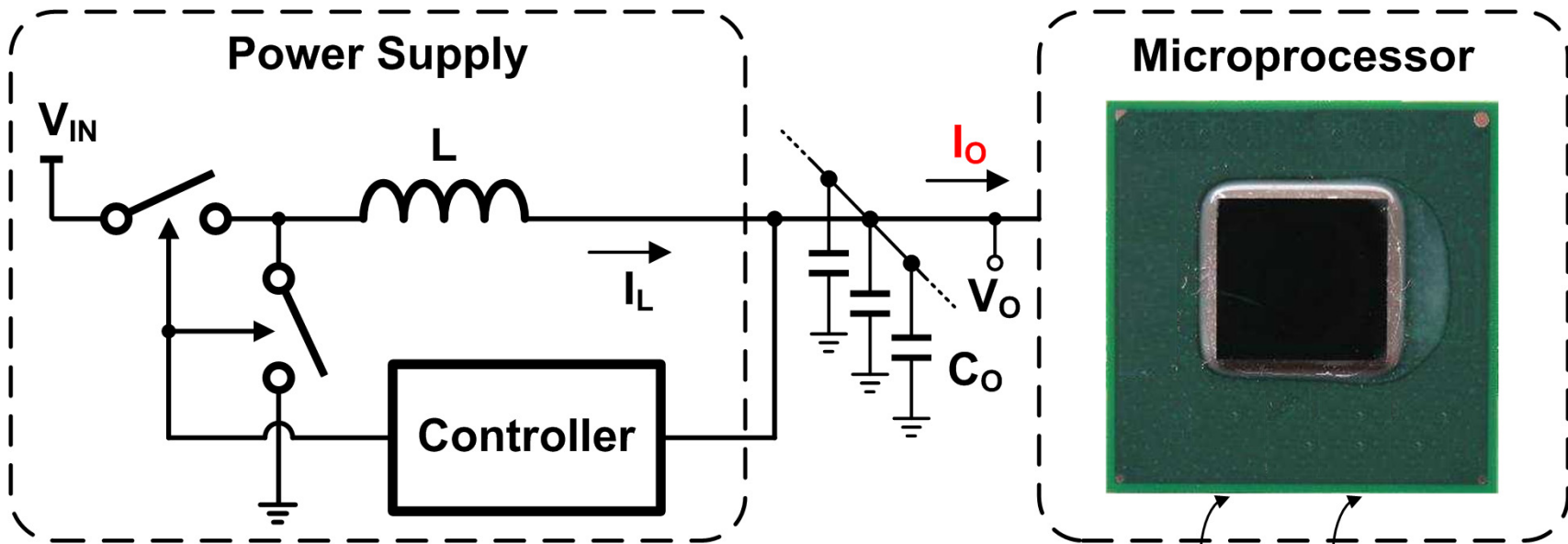
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- **Background and Challenges**
- **Proposed Design**
 - **Control Scheme : Zero Delay Response**
 - **Control Scheme : f_{sw} Synchronization**
 - **Emulated AC+DC Current Sensing**
 - **Wide Range Efficiency**
- **Four-Phase System Architecture**
- **Measurement Results**
- **Comparison and Conclusion**

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Microprocessor Power Supply Trends

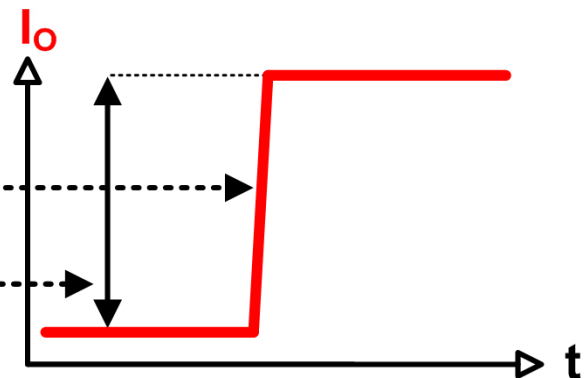


Recent Trends:

- Increasing clock frequency.
- Greater number of cores.
- Increasing power dissipation.

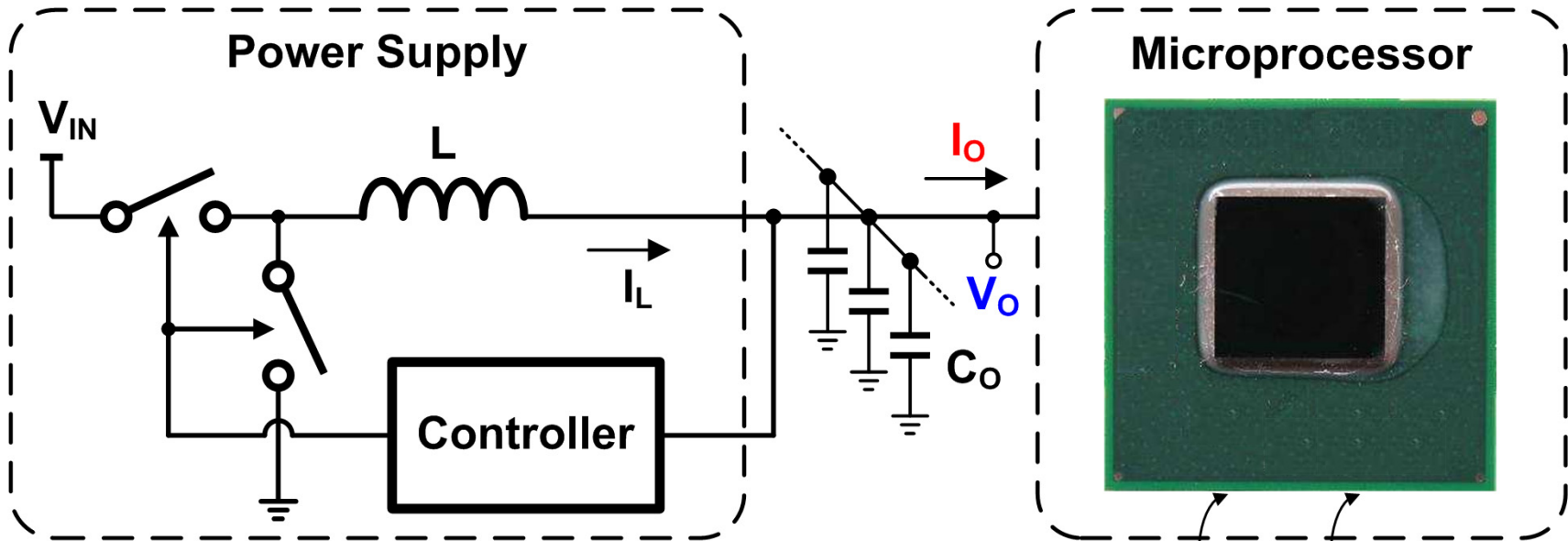
*Fast Slew
Rate: $>1A/ns$*

*Extremely High
Magnitude*



More cores! Faster CLK!

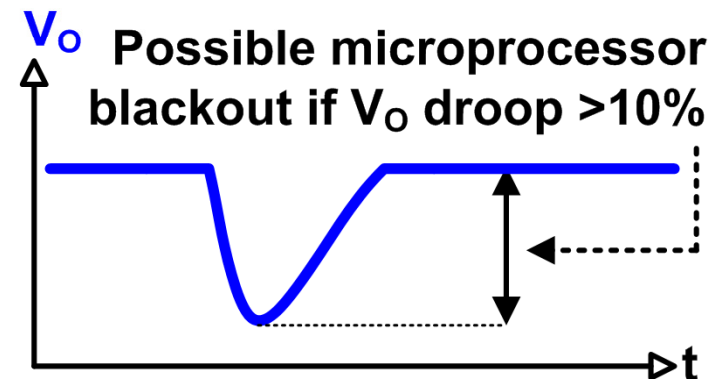
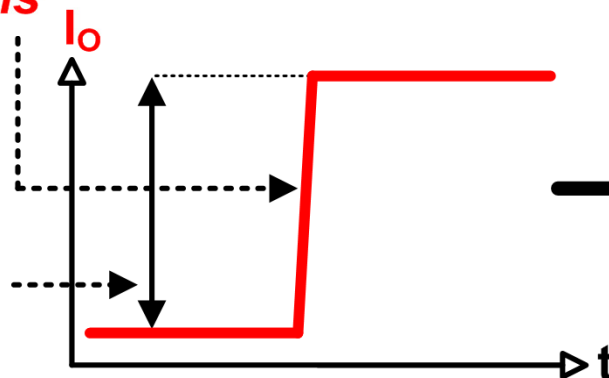
Microprocessor Power Supply Trends



Fast Slew

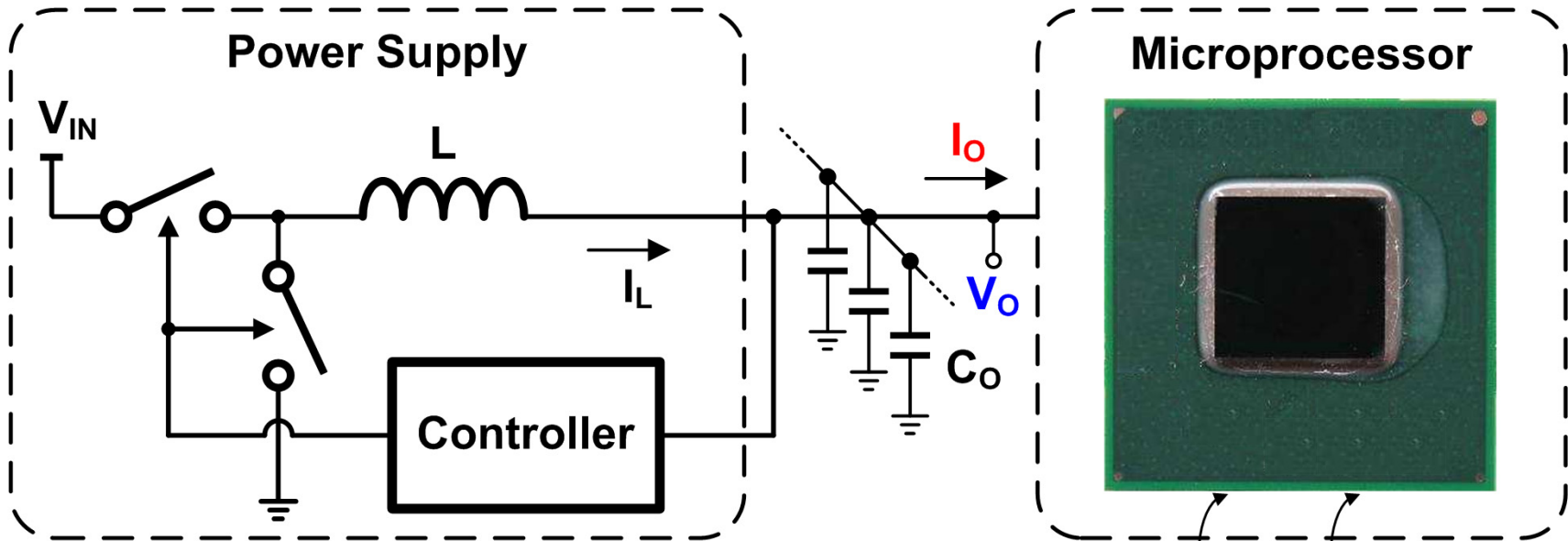
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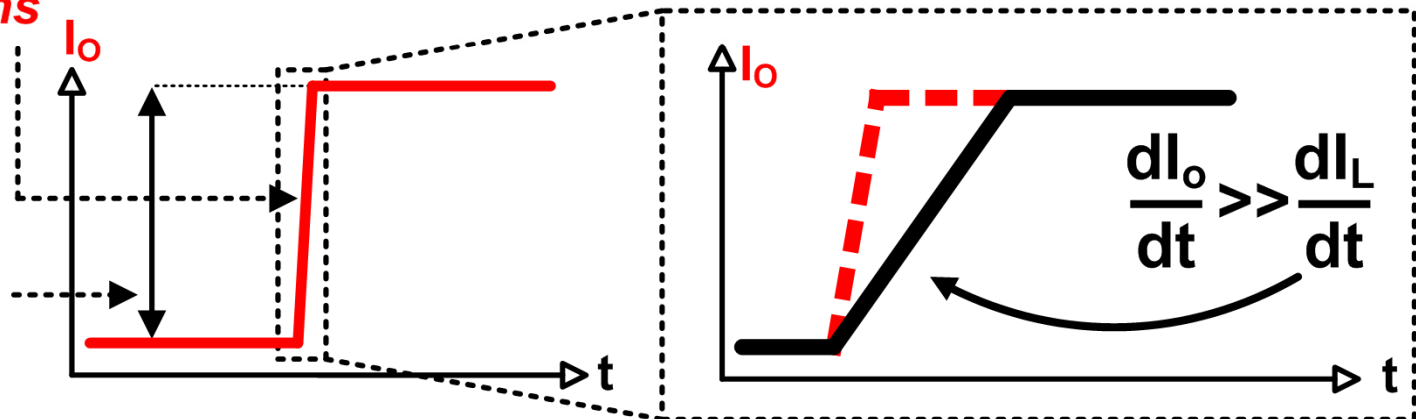
Major Challenges



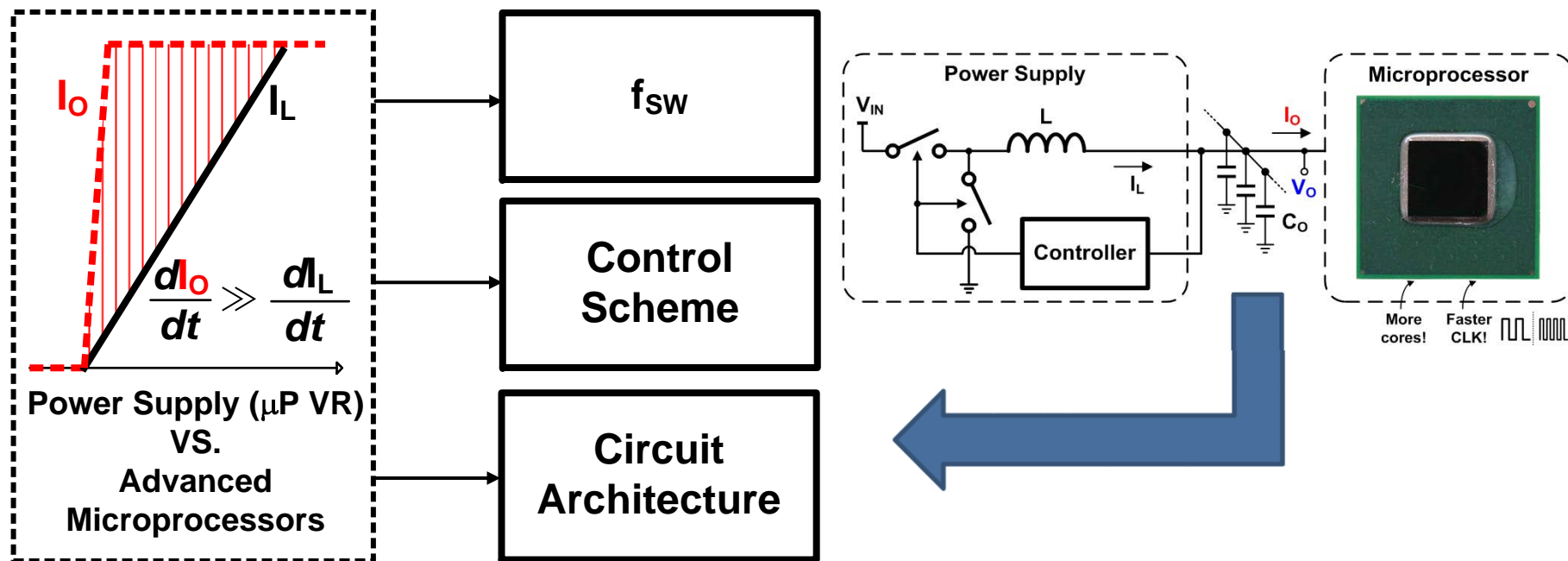
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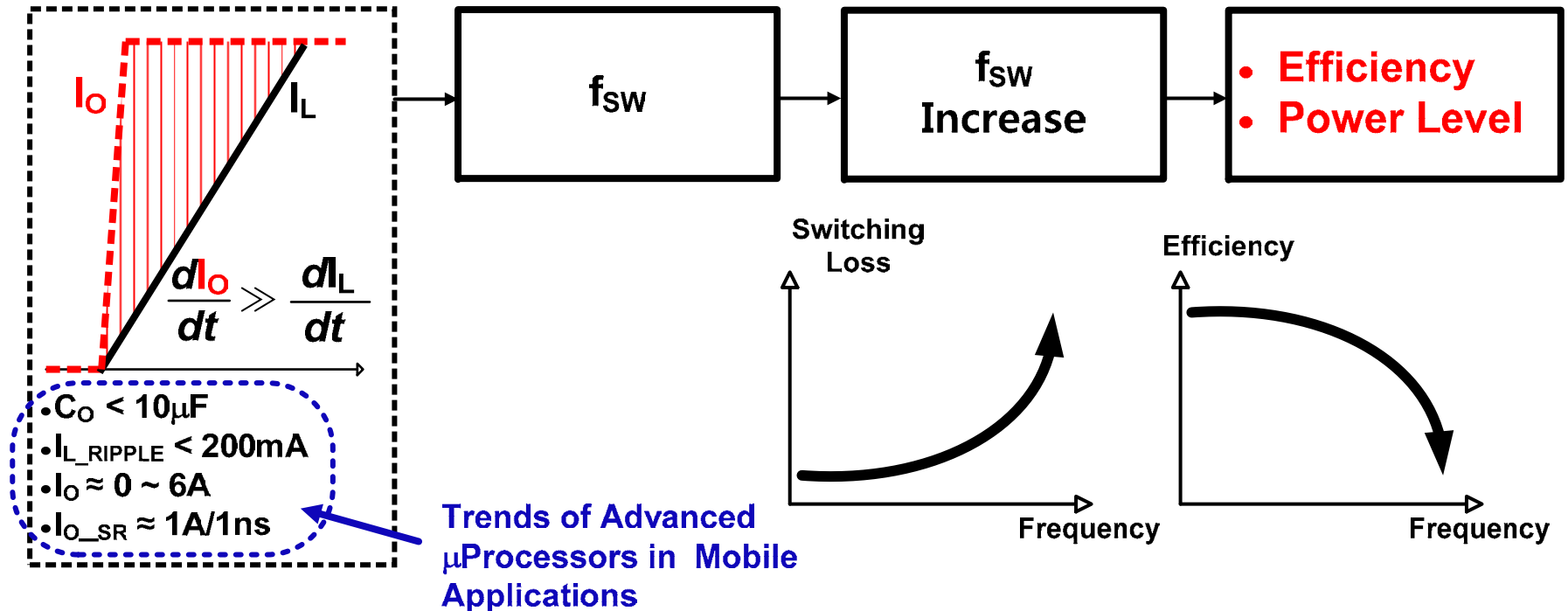
Major Challenges : Design Aspects



• Key Design Considerations

- f_{sw} Increase – *Faster response.*
- Control Scheme – *Fast feedback loop regulation.*
- Circuit Architecture – *Physical dI_L/dt limit, Wide range efficiency.*

Key Design Consideration: f_{sw}

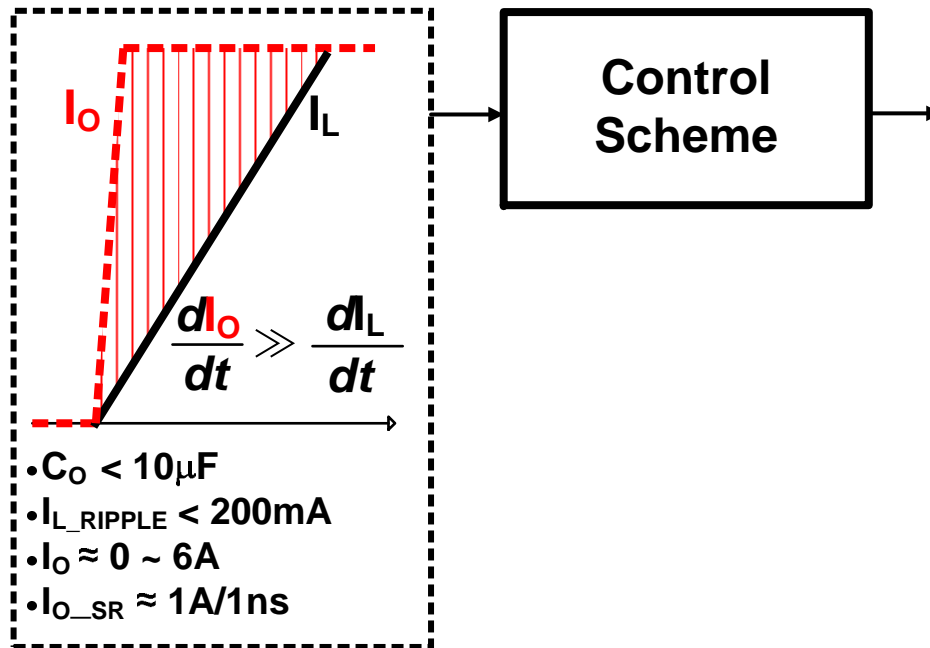


- f_{sw} Increase

- To satisfy the Trends: $f_{sw} \approx 0.5 \sim 1GHz^*$
- Dramatic switching power loss increase.
- Limits on high voltage and high current implementation.

* P. Hazucha et al., "A 233-MHz 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 838-845, Apr. 2005.

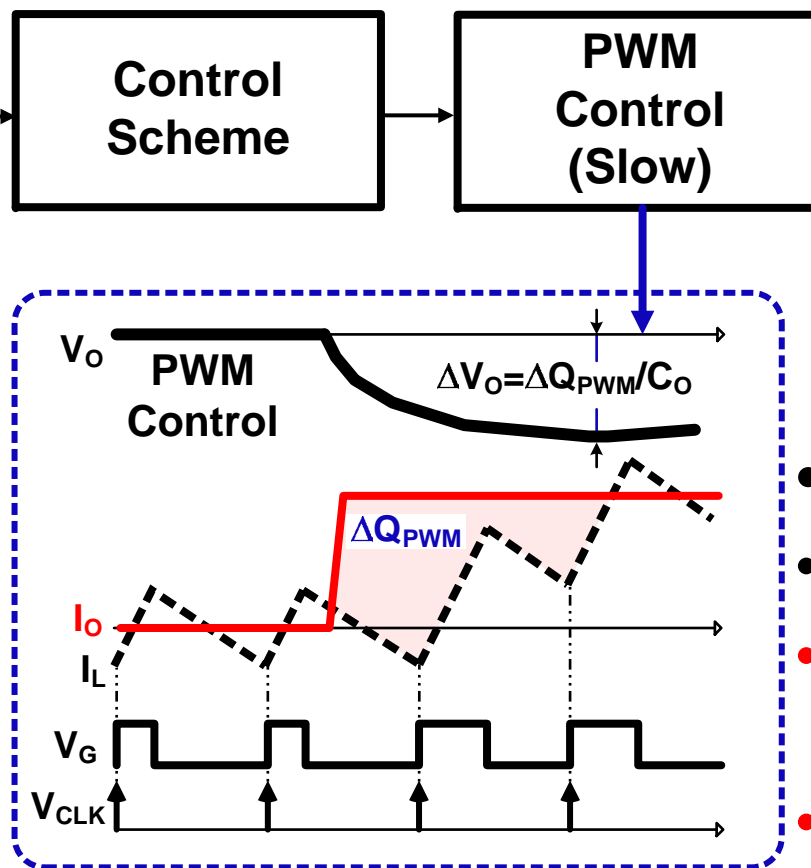
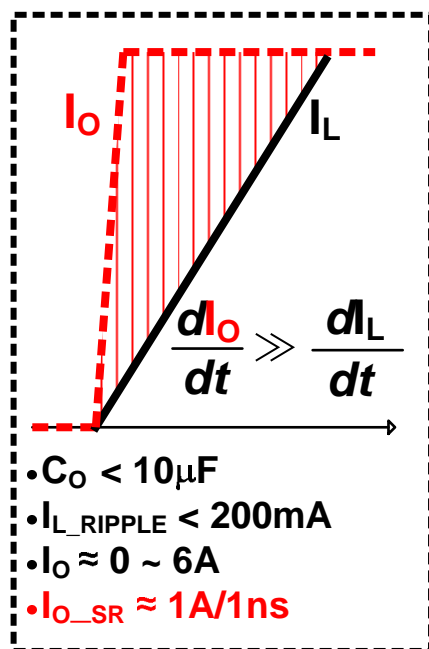
Key Design Consideration: Control Scheme



- **Control Scheme**

- Fast or slow feedback loop for regulation under extreme load transients.
- Fixed (synchronized) or varying f_{sw} .

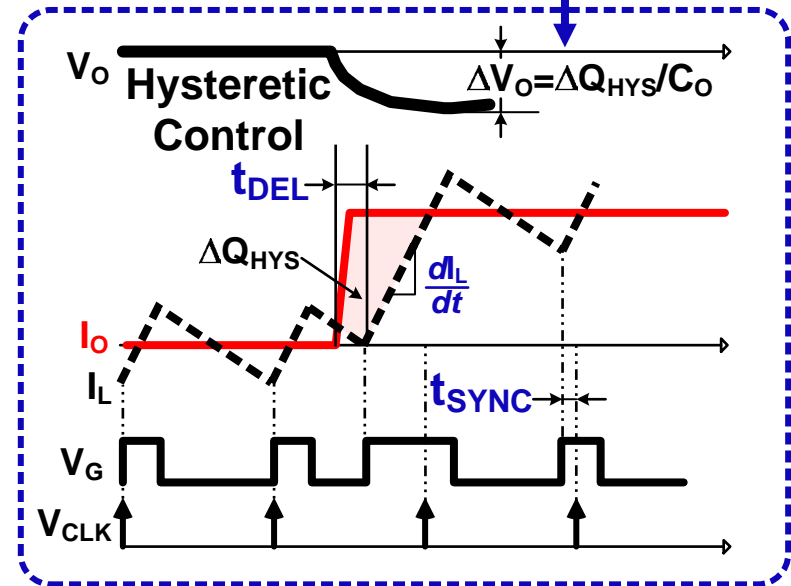
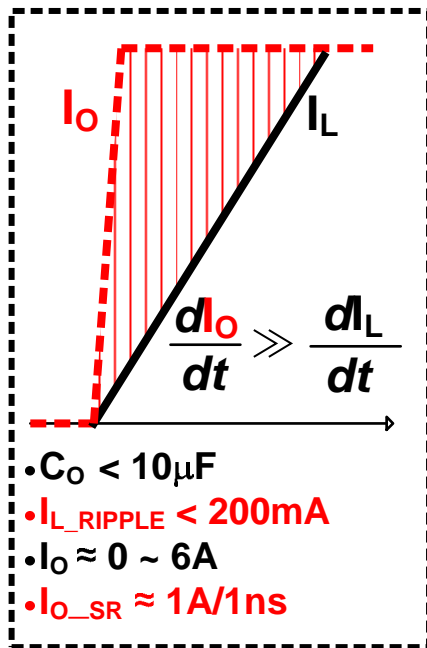
Key Design Consideration: Control Scheme



- PWM Control
- Fixed f_{SW} .
- Slow feedback loop.* $-\Delta Q_{PWM}$
- Larger V_O droop.

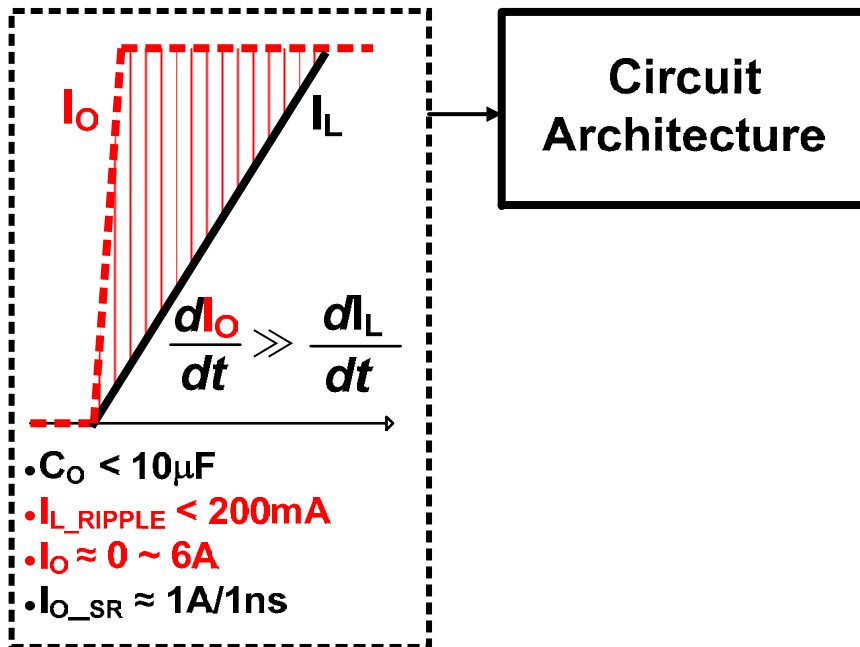
* C. Huang and P. K. T. Mok, "An 82.4% Efficiency Package-Bondwire-Based Four-Phase Fully Integrated Buck Converter with Flying Capacitor for Area Reduction," IEEE ISSCC Dig. Tech. Papers, pp. 362-364, Feb. 2013.

Key Design Consideration: Control Scheme



- **Hysteretic Control**
- **Fast response.**
- **Still, hysteresis delay. – t_{DEL}**
- **Varying f_{sw} . – t_{SYNC}**
- **Physical inductor current slew rate limitation. – dI_L/dt**

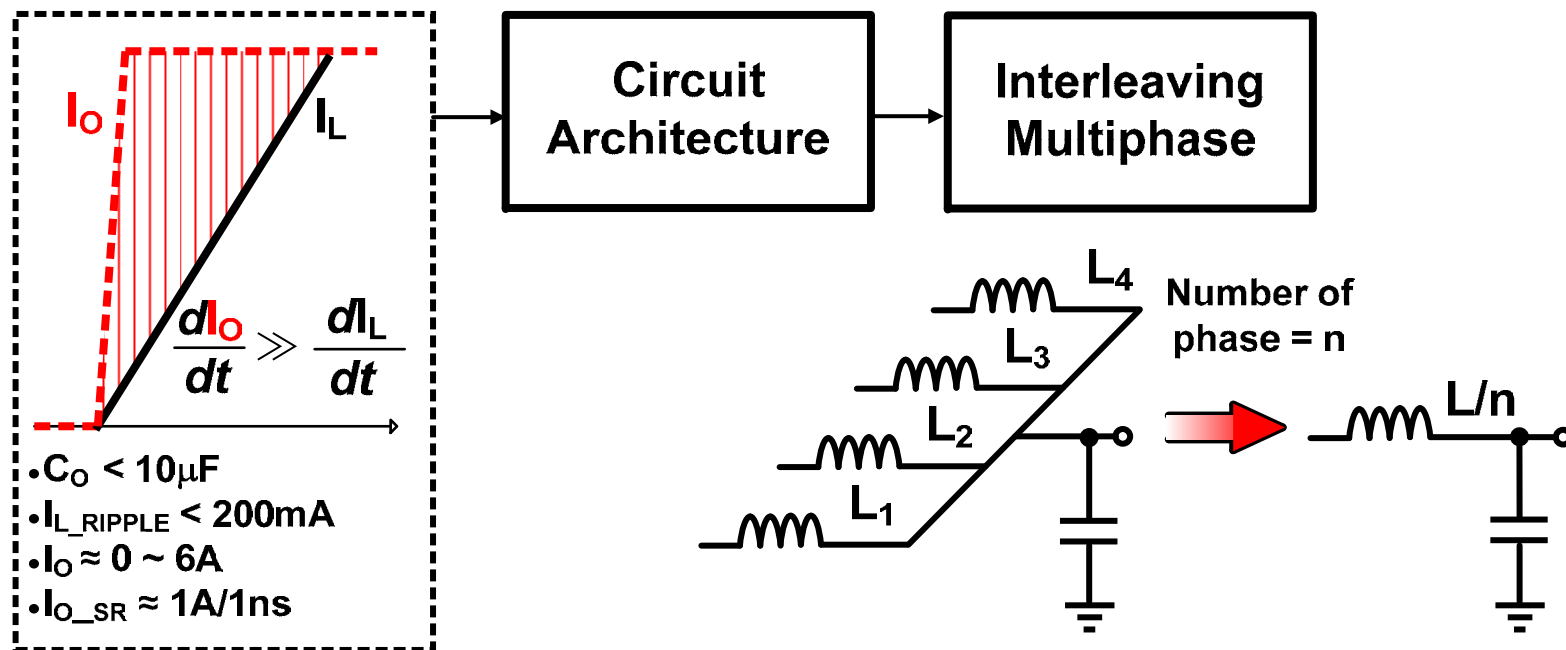
Key Design Consideration: Circuit Architecture



- **Circuit Architecture**

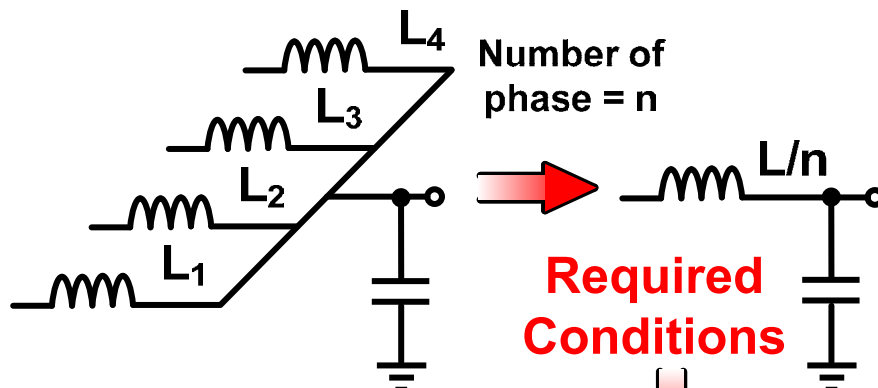
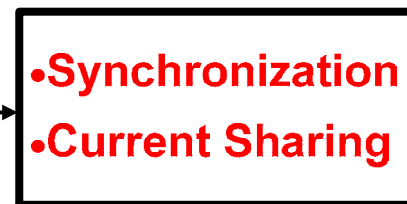
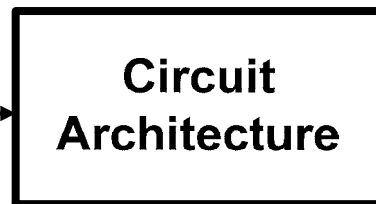
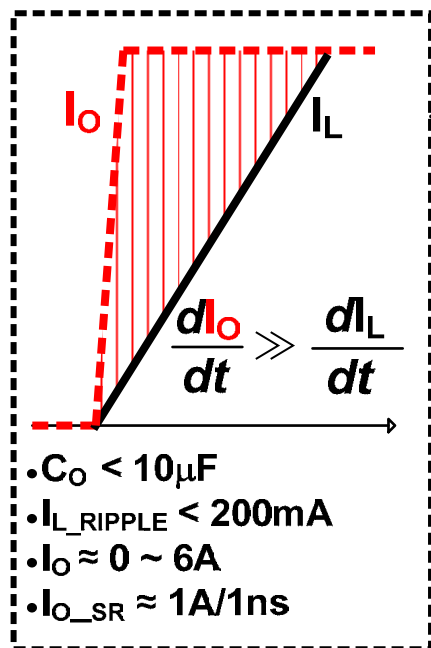
- How to solve physical inductor current slew rate limitation?
- How to achieve efficiency over wide range of load?
- How to maximize power level?
- How to realize very high f_{sw} operation and current sensing?

Key Design Consideration: Circuit Architecture



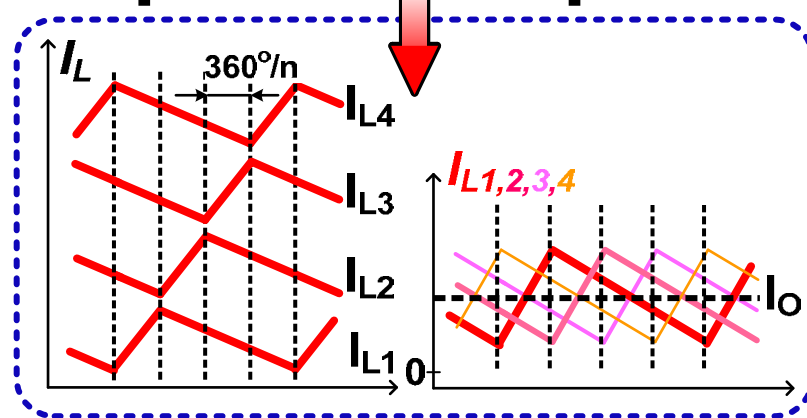
- **Multiphase Implementation Benefits**
 - Physical I_L slew rate increase.
 - Bandwidth increase.
 - Power level increase.

Key Design Consideration: Circuit Architecture



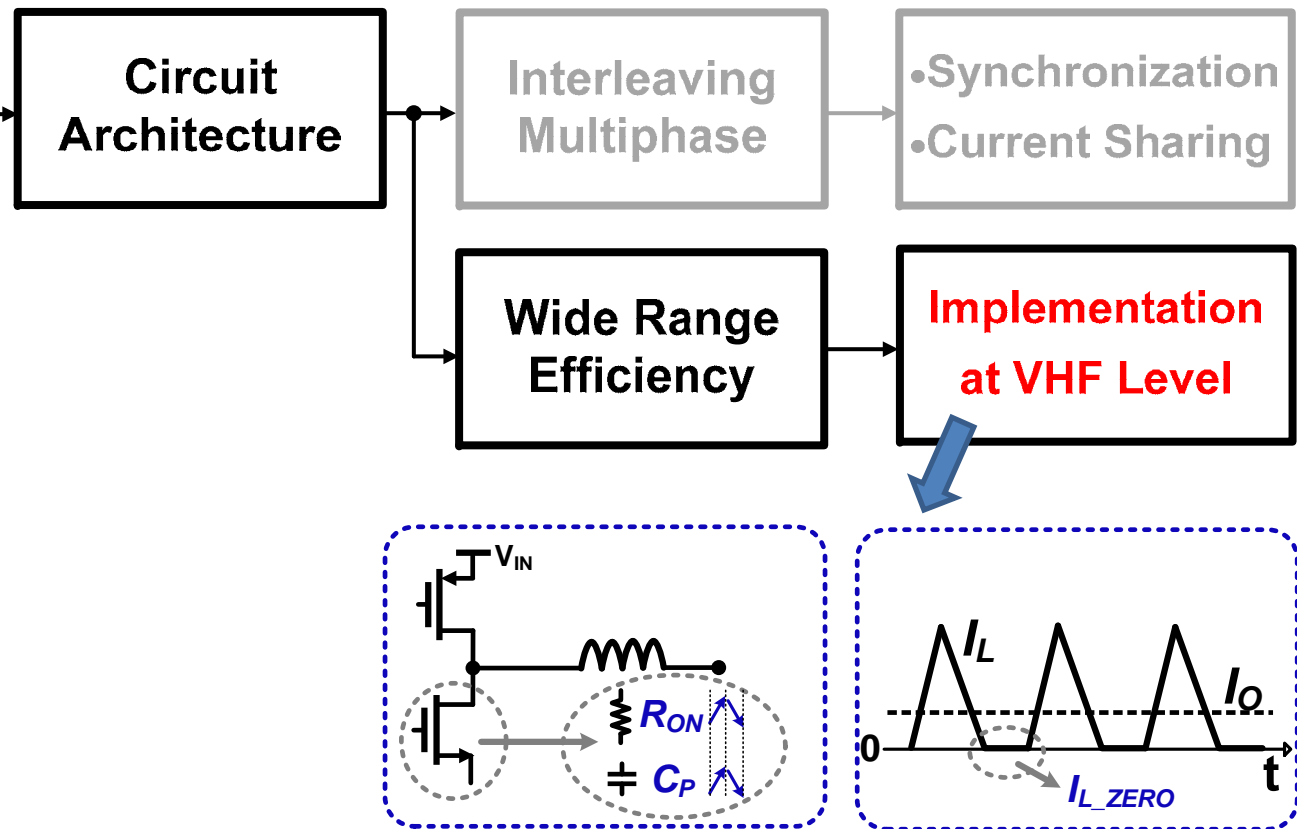
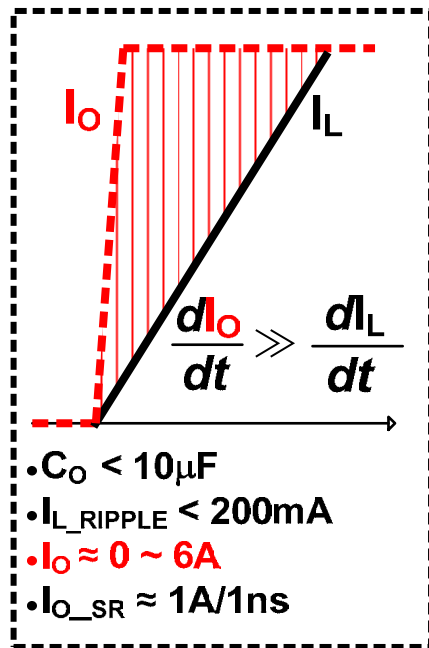
• Challenges

- Synchronization, current-sharing* along with *fast hysteretic control*.
- Circuit implementation of current sensing at VHF levels.



* P. Li et al., "A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3131-3145, Nov. 2009.

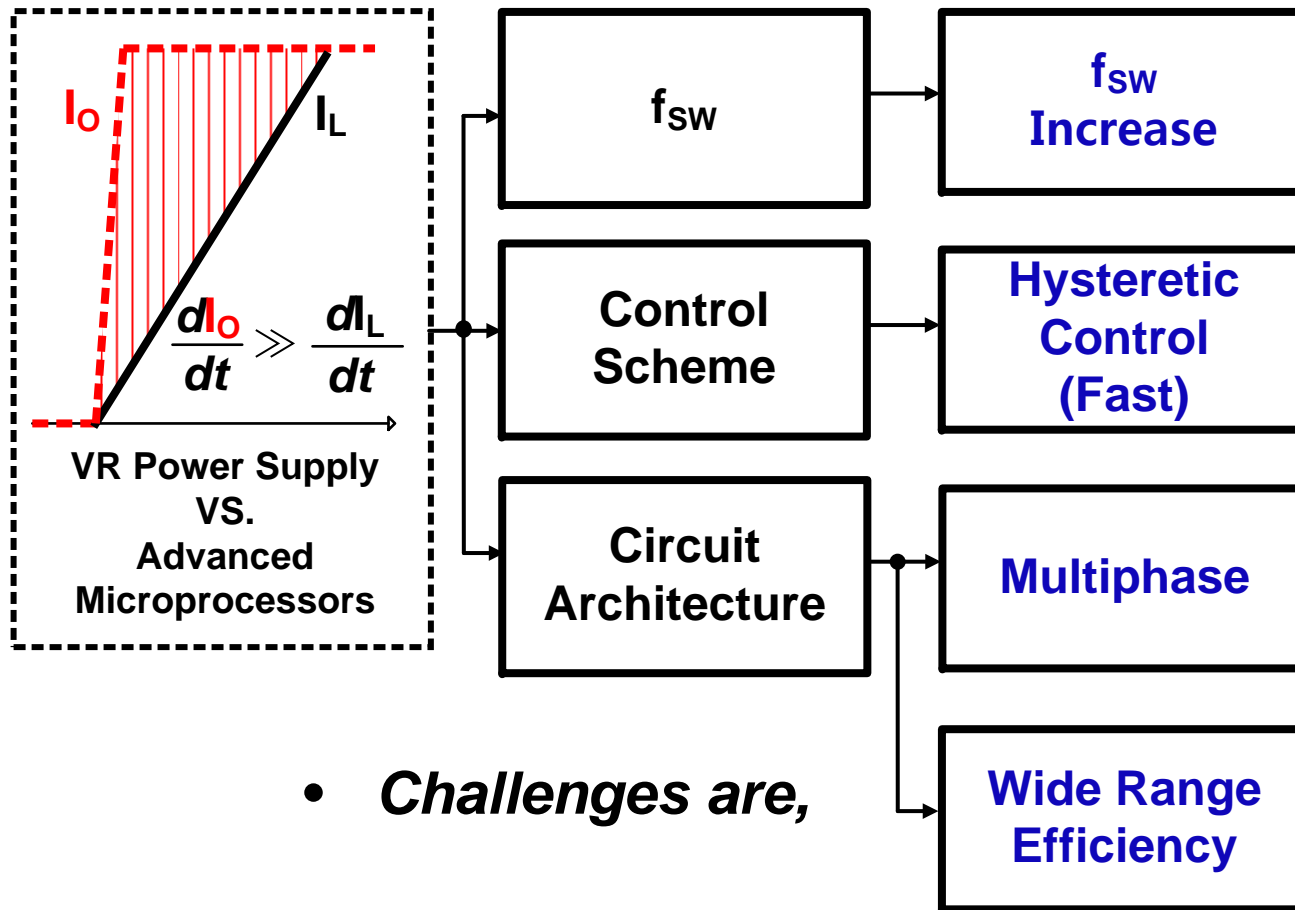
Key Design Consideration: Circuit Architecture



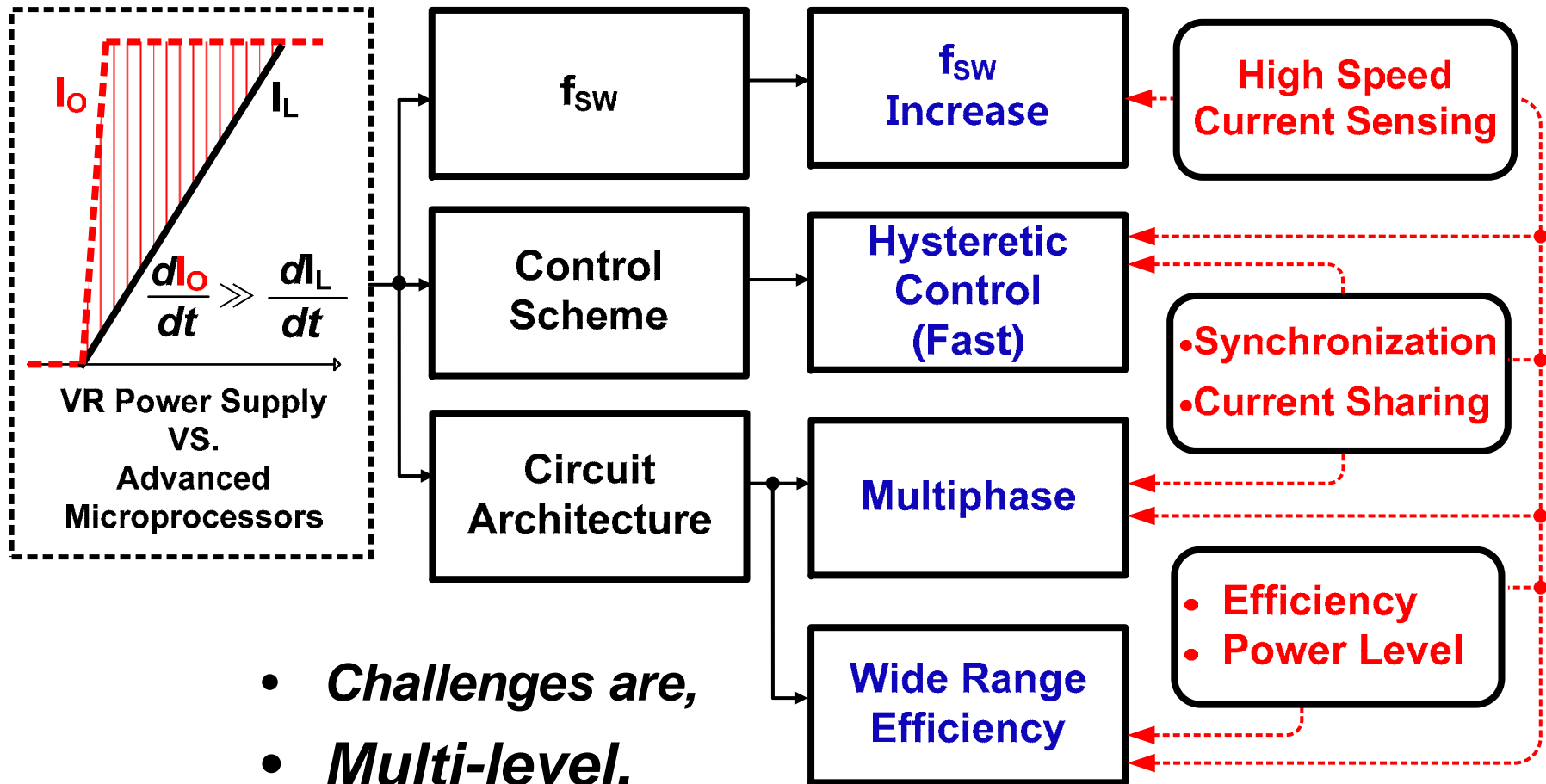
Challenges

- Very high f_{sw} operation and circuit implementation.
- Accurate I_L current sensing at very high f_{sw} .

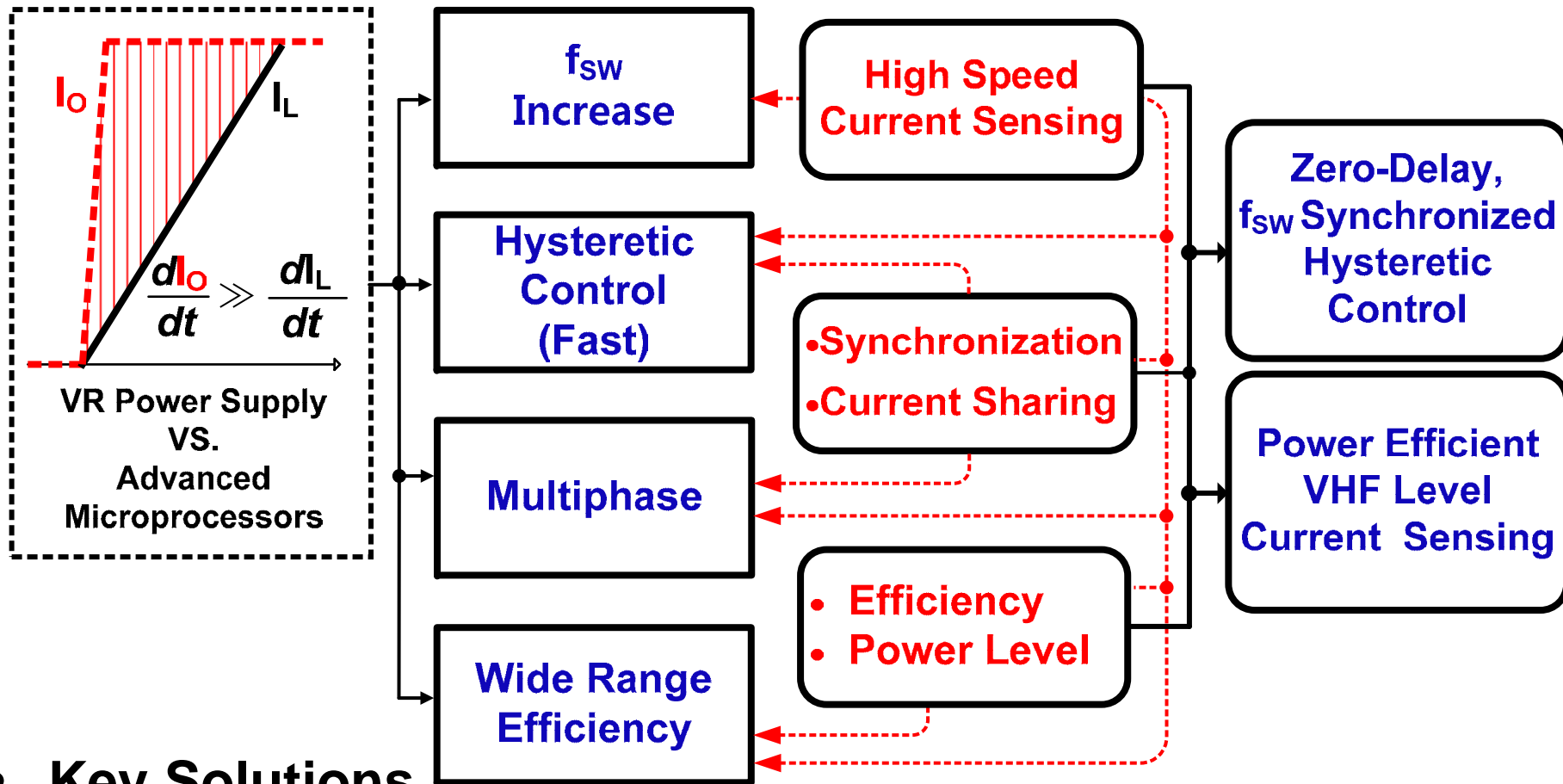
Summary of Major Challenges



Summary of Major Challenges



Proposed Design

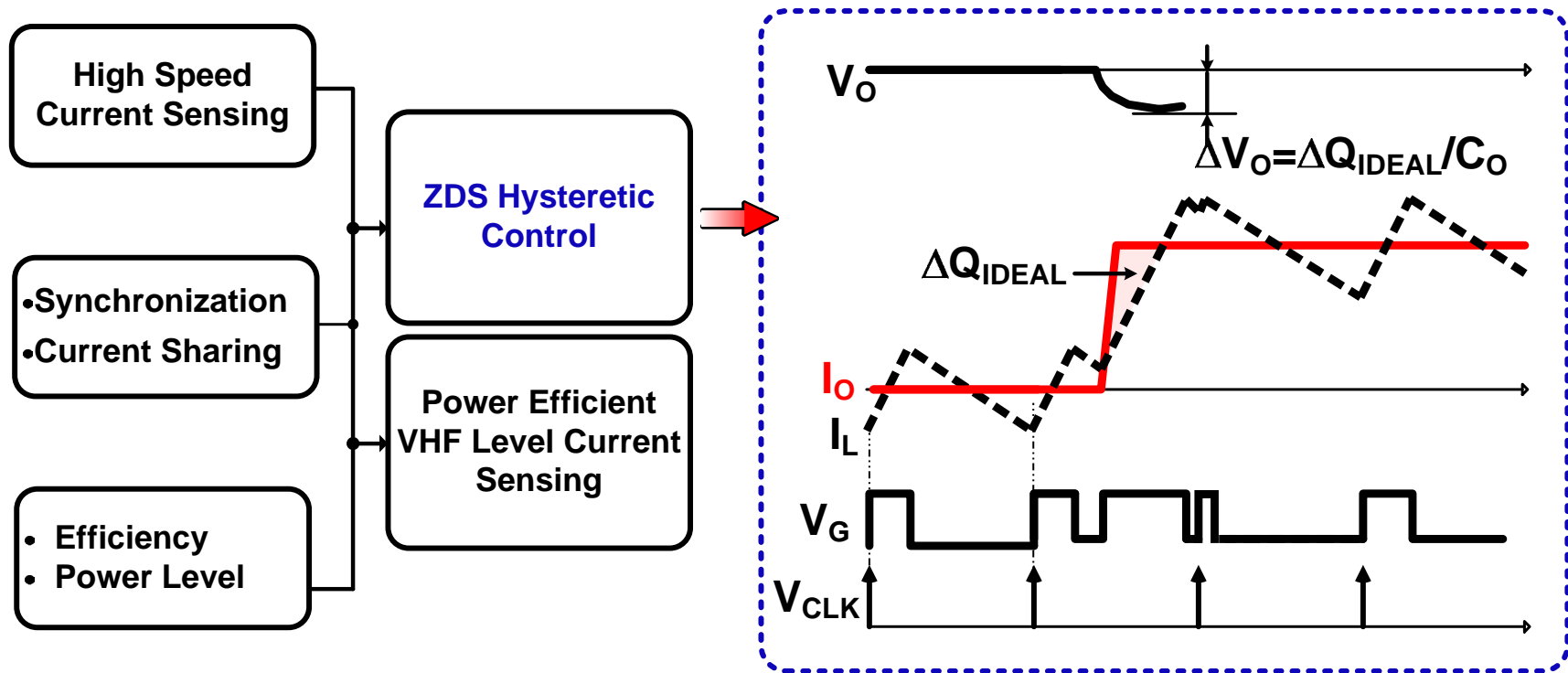


- **Key Solutions**
- New control scheme achieving zero-delay response and synchronized f_{sw} operation simultaneously.
- Technique for low power, very high speed current sensing.

Outline

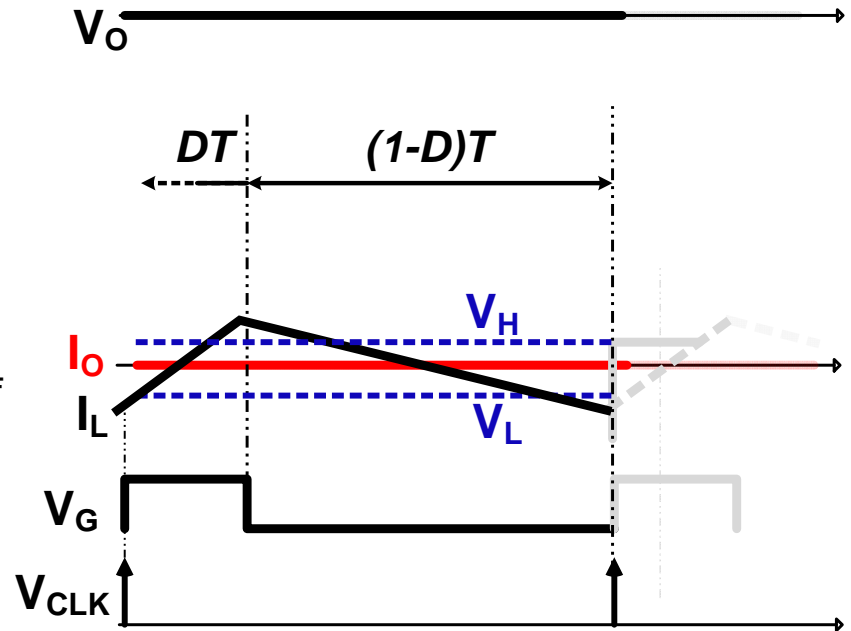
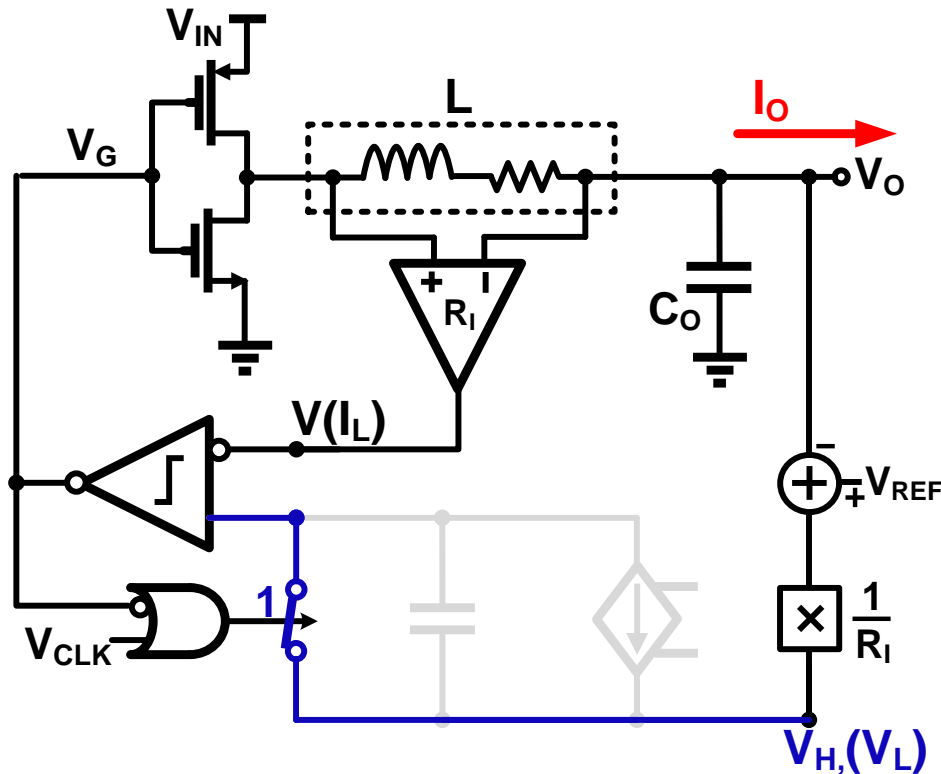
- Background and Challenges
- **Proposed Design**
 - **Control Scheme : Zero Delay Response**
 - Control Scheme : f_{sw} Synchronization
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Key Features of ZDS Hysteretic Control



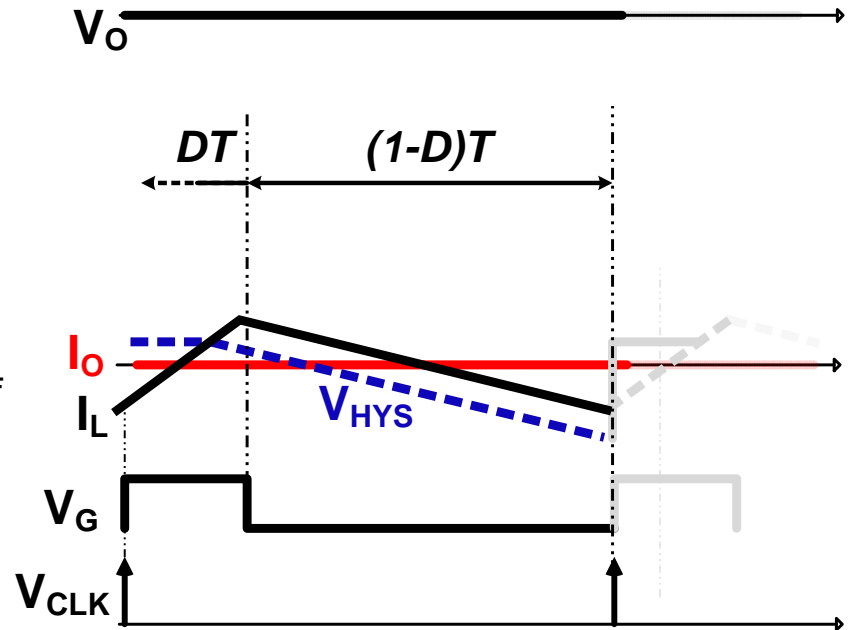
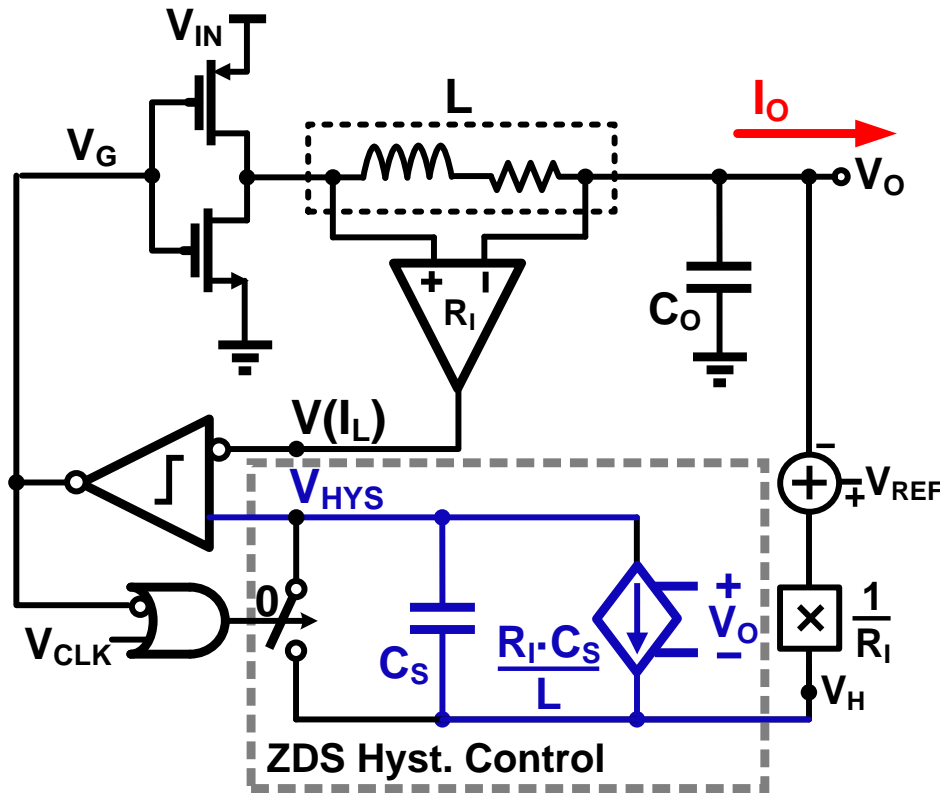
- **Zero-Delay Synchronized Hysteretic Control**
 - *Near-zero delay hysteretic response to load transients.*

Drawbacks in Normal Hysteretic Control



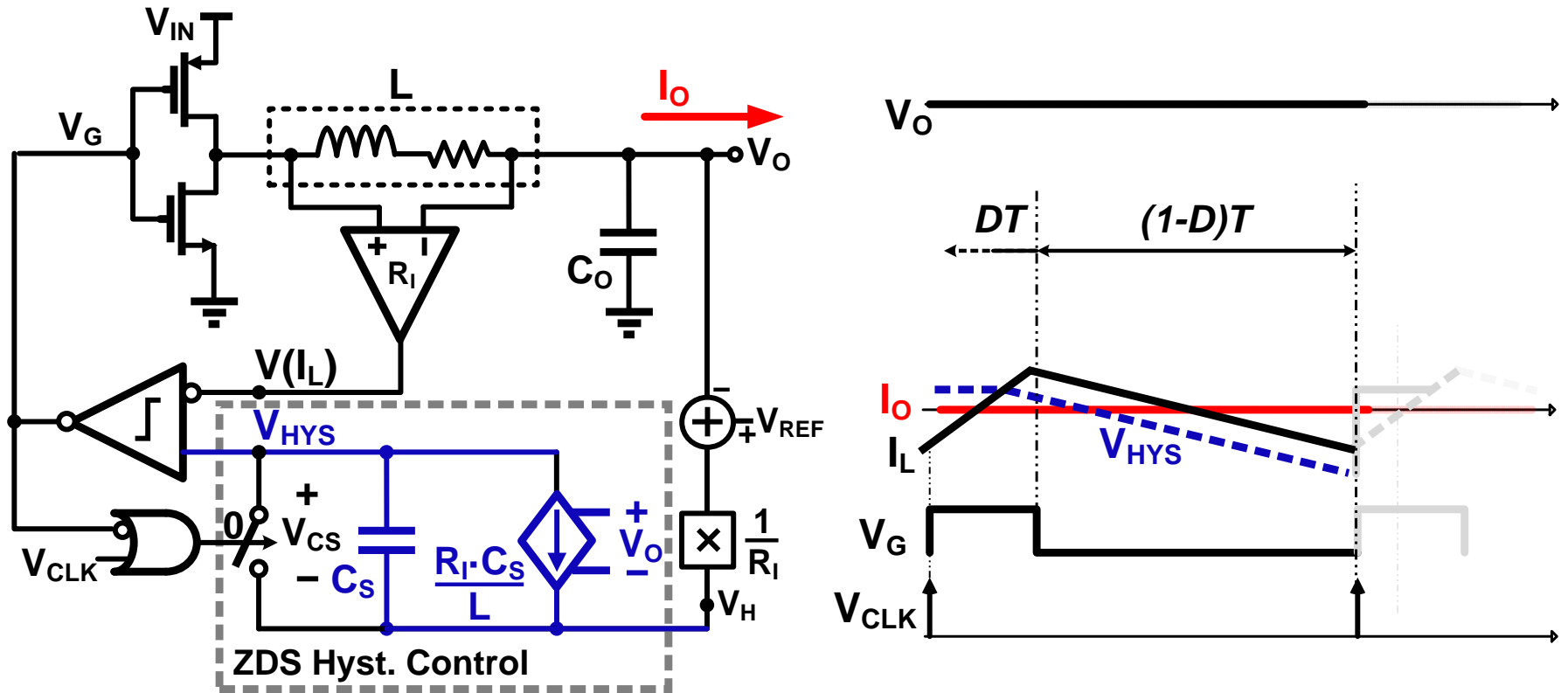
- Fixed Hysteresis Window
 - Finite hysteresis window size of $V_H - V_L$.
 - Hysteresis delay $\propto V_H - V_L$.

Proposed ZDS Hysteretic Control



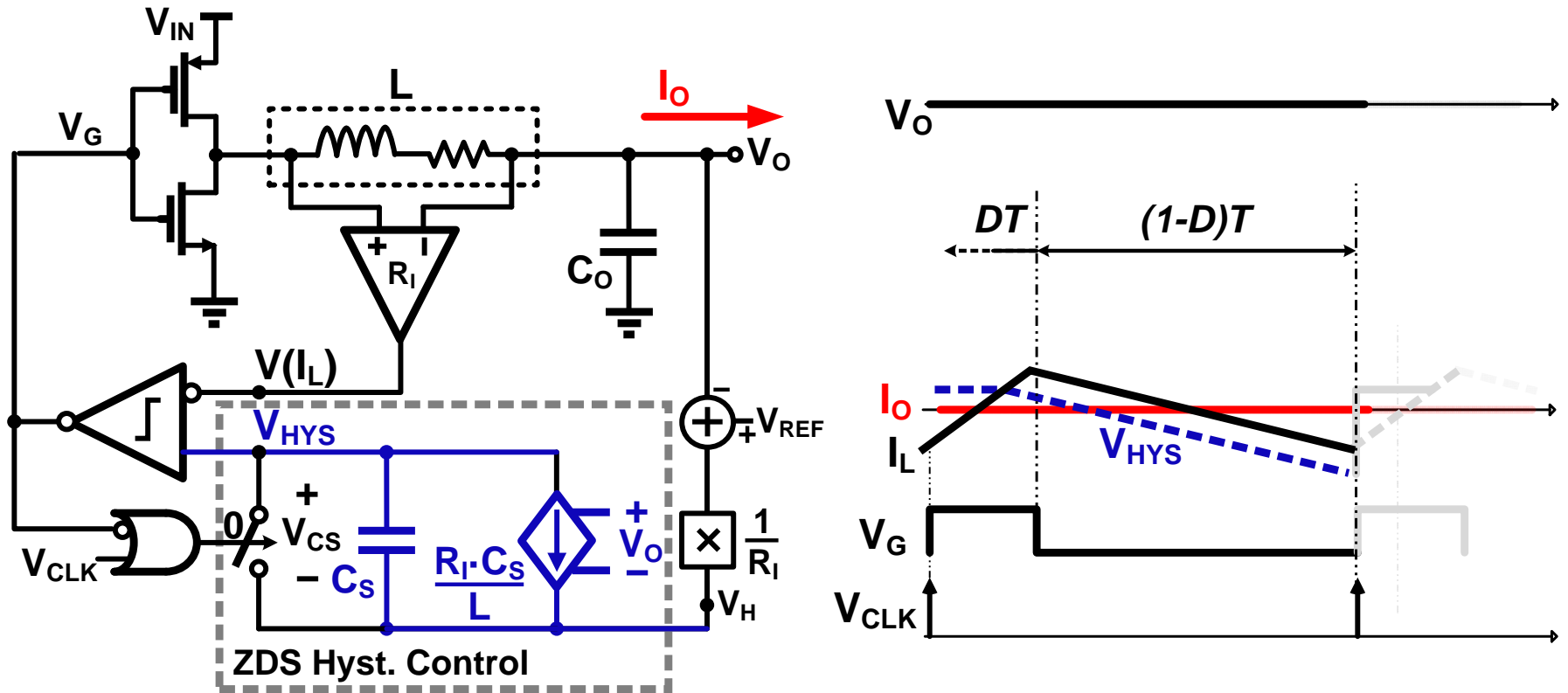
- **Fixed Hysteresis Window**
 - Finite hysteresis window size of $V_H - V_L$.
 - Hysteresis delay $\propto V_H - V_L$.
- **Adaptive Hysteresis Window**
 - I_L -tracking hysteretic reference, V_{HYS} .
 - **ZERO** hysteresis delay.

Control Scheme: Zero Delay Response



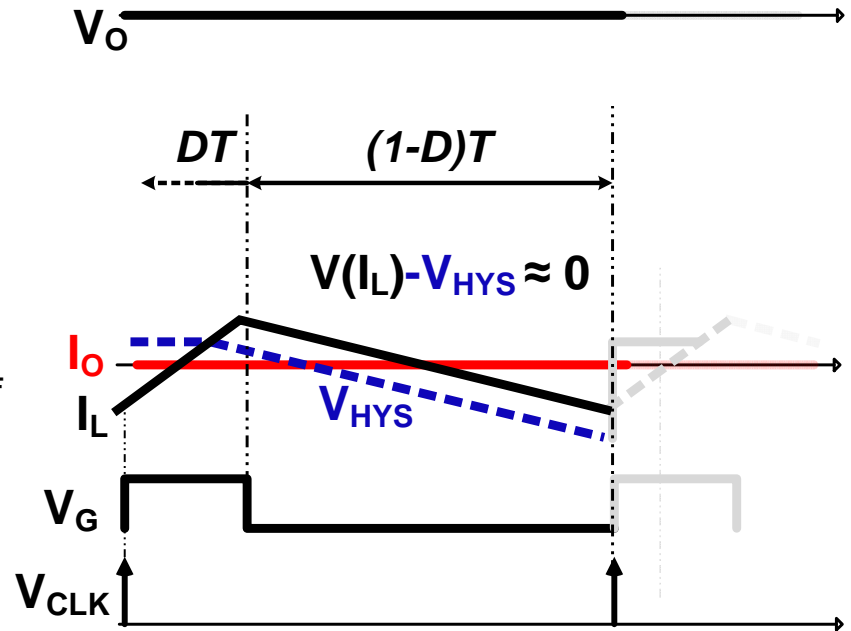
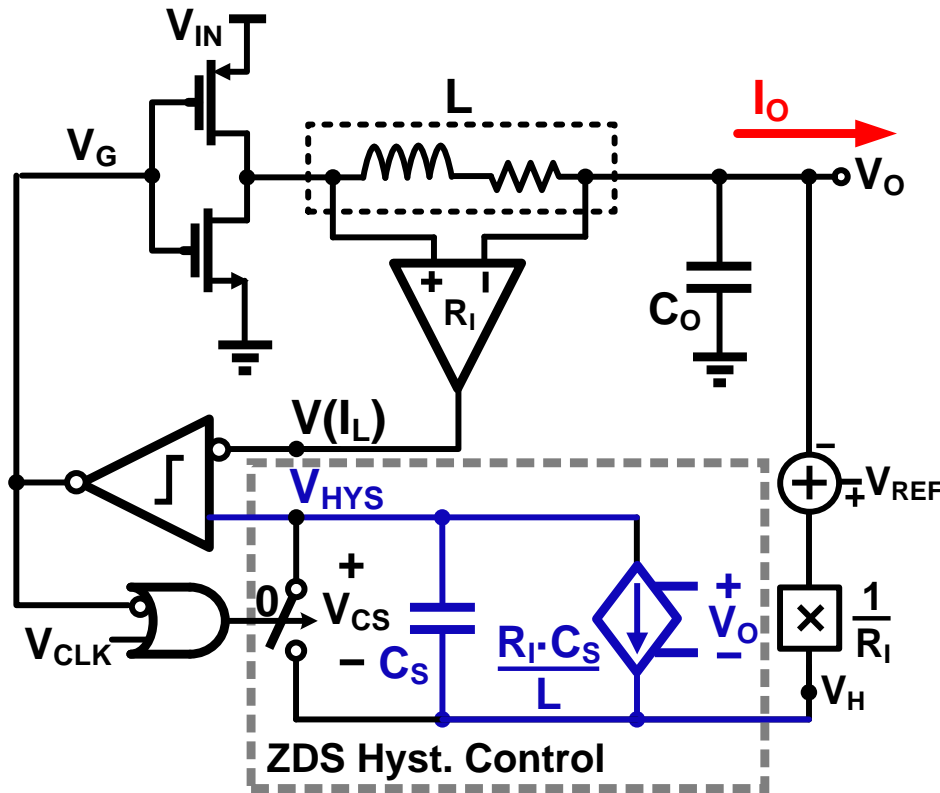
- During $(1-D)T$, C_S is linearly discharged by a V_O -dependent I source, creating $V_{CS} = R_I \times V_O / L$.

Control Scheme: Zero Delay Response



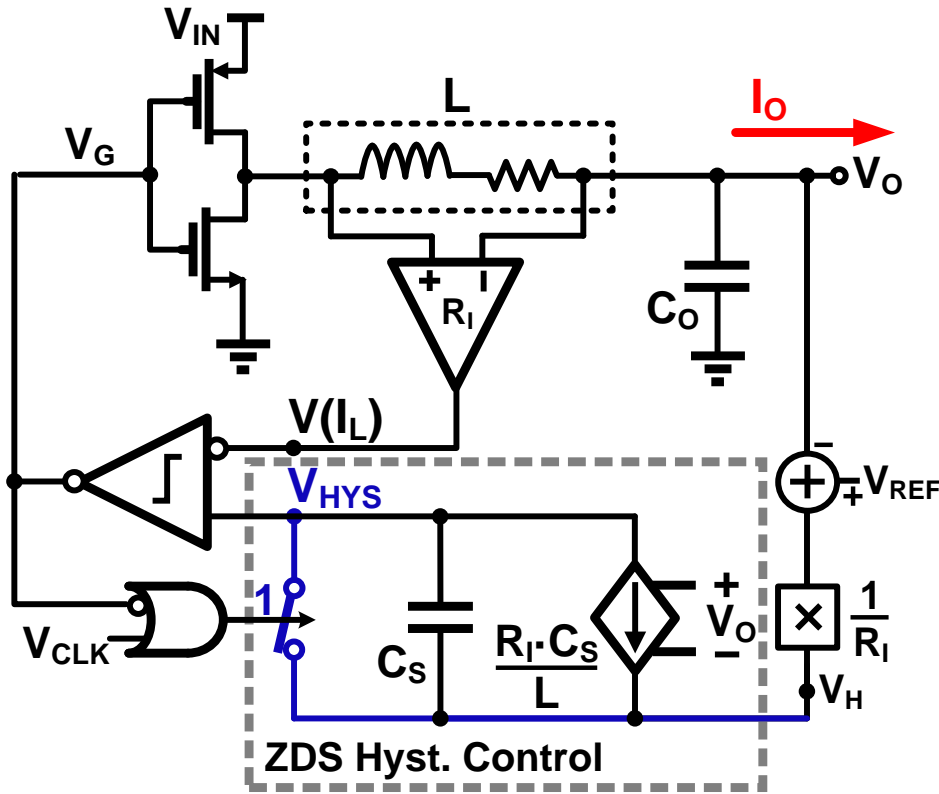
- During $(1-D)T$, C_S is linearly discharged by a V_O -dependent I source, creating $V_{CS} = R_I \times V_O / L$.
- By $V_H - V_{CS}$, ΔI_L -tracking hysteresis reference V_{HYS} is created.

Control Scheme: Zero Delay Response

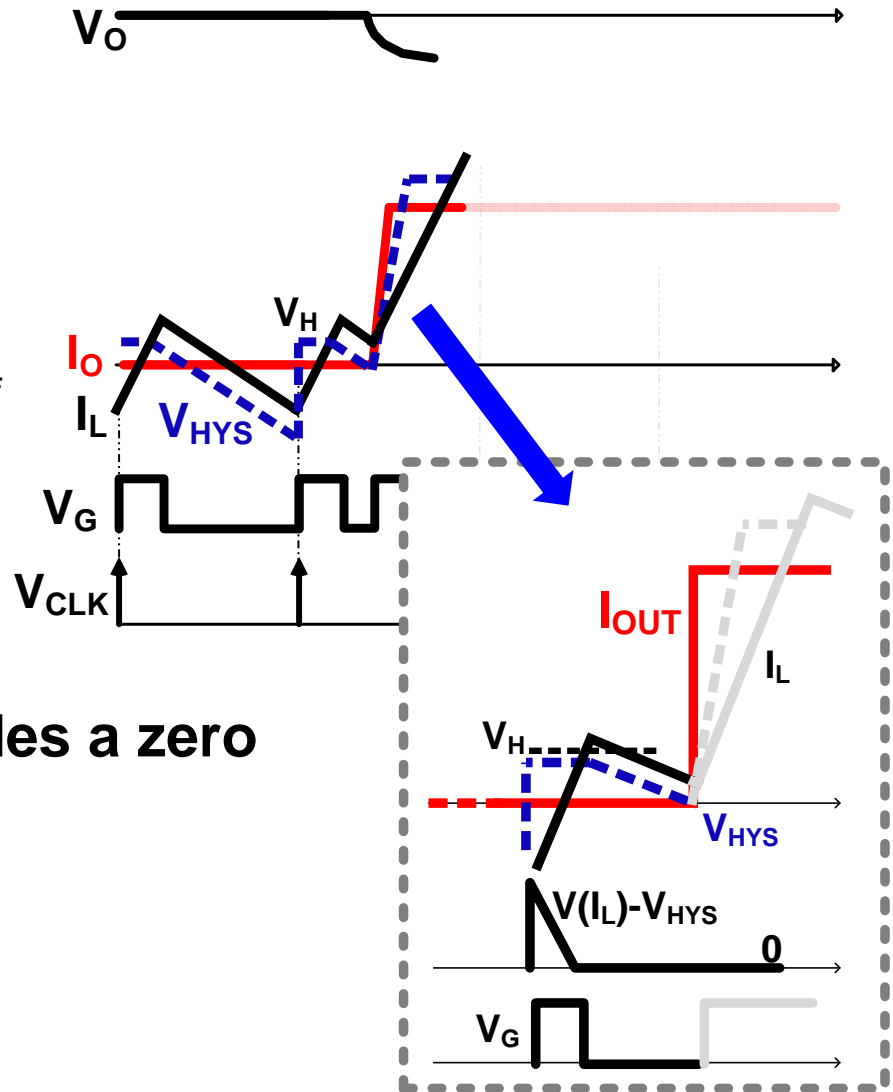


- During $(1-D)T$, C_S is linearly discharged by a V_O -dependent I source, creating $V_{CS} = R_I \times V_O / L$.
- By $V_H - V_{CS}$, ΔI_L -tracking hysteresis reference V_{HYS} is created.
- Since V_{HYS} is tracking down with I_L , a near zero hysteresis window is achieved.

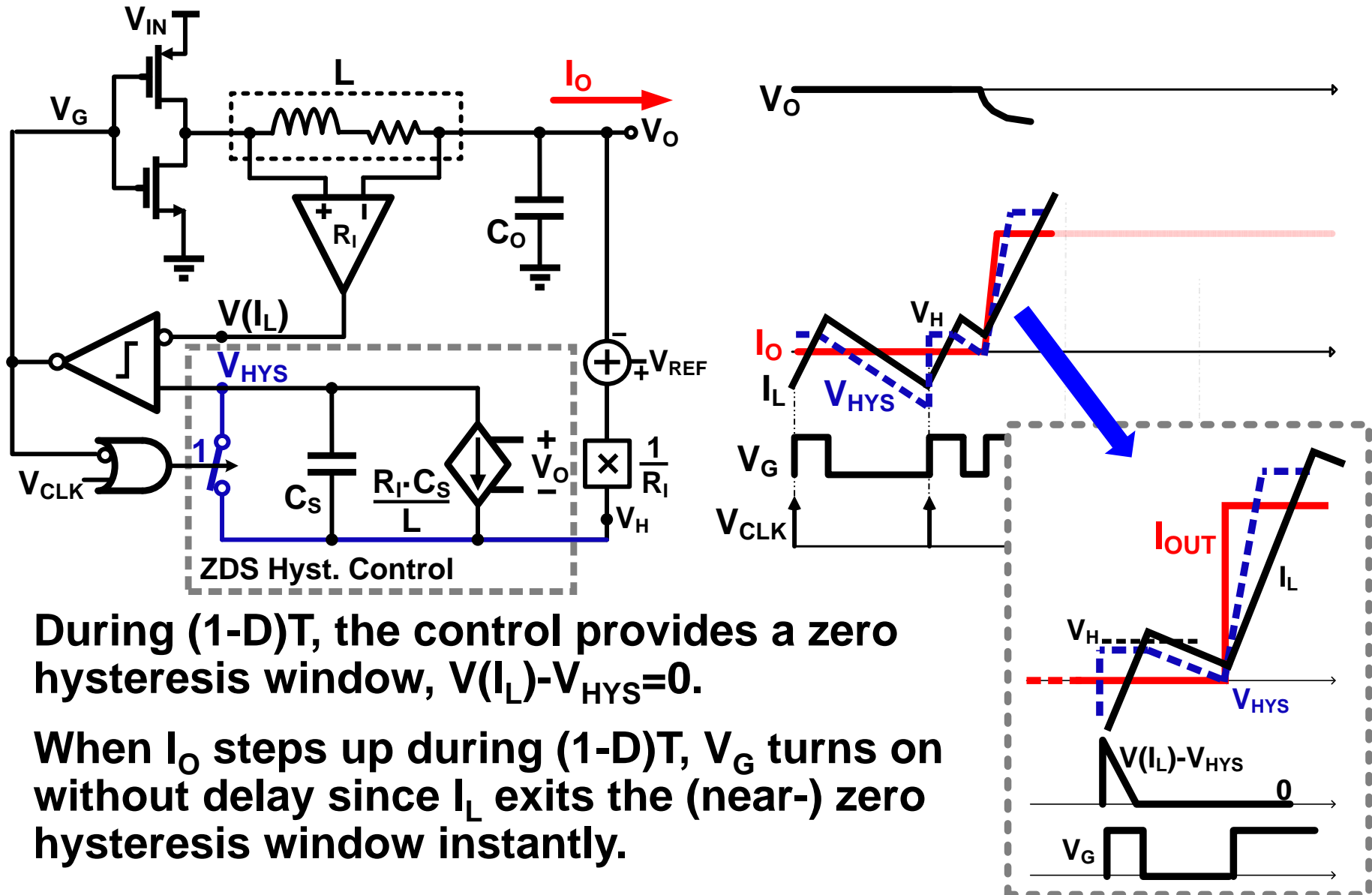
Zero Delay Response at I_0 Step-Up



- During (1-D)T, the control provides a zero hysteresis window, $V(I_L) - V_{HYS} = 0$.



Zero Delay Response at I_o Step-Up

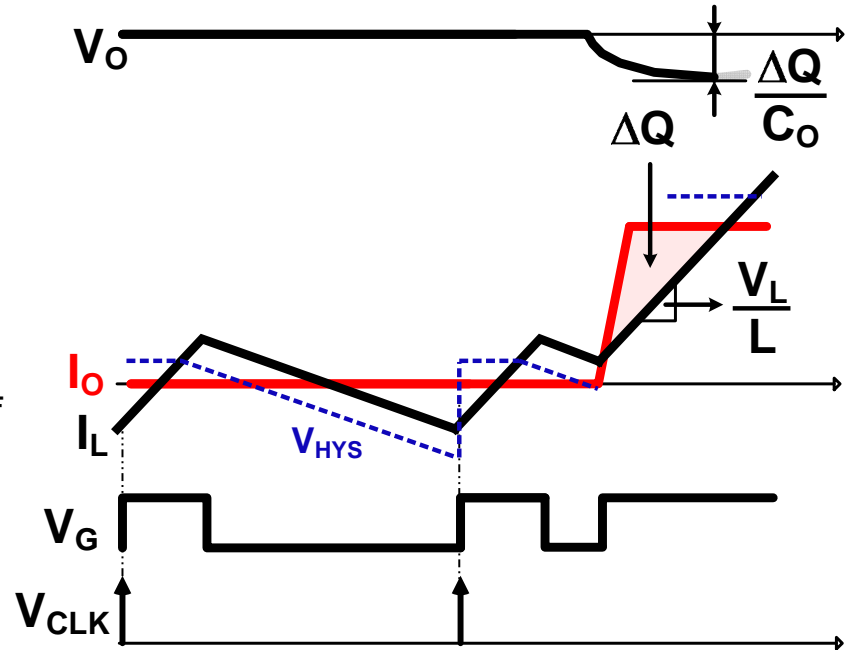
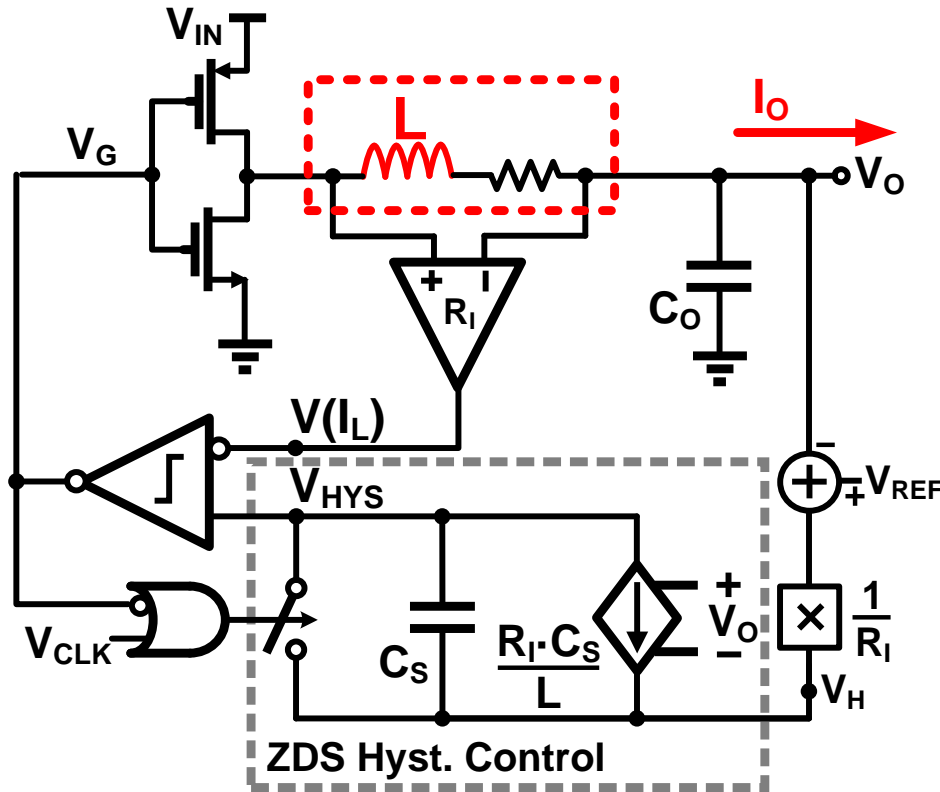


- During (1-D)T, the control provides a zero hysteresis window, $V(I_L) - V_{HYS} = 0$.
- When I_o steps up during (1-D)T, V_G turns on without delay since I_L exits the (near-) zero hysteresis window instantly.

Outline

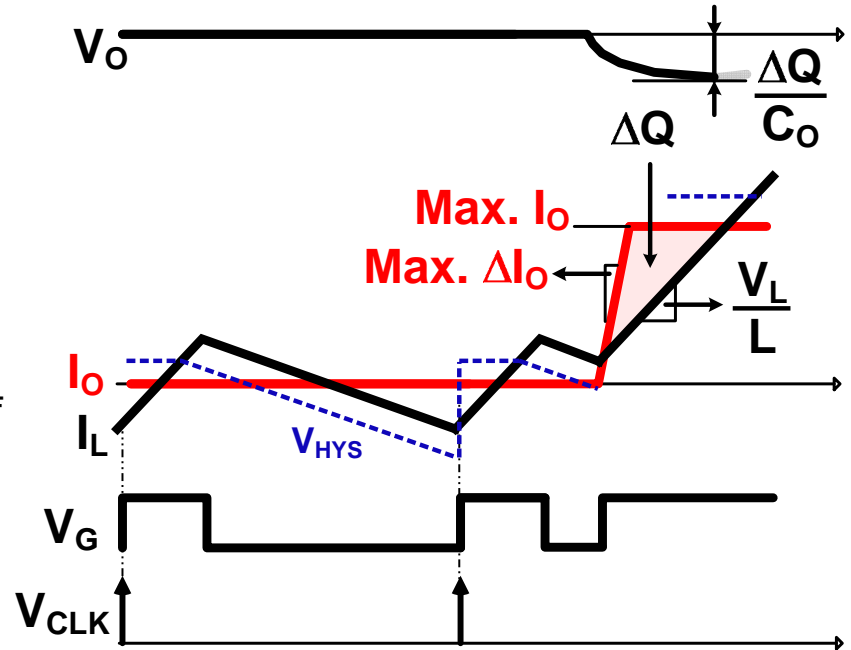
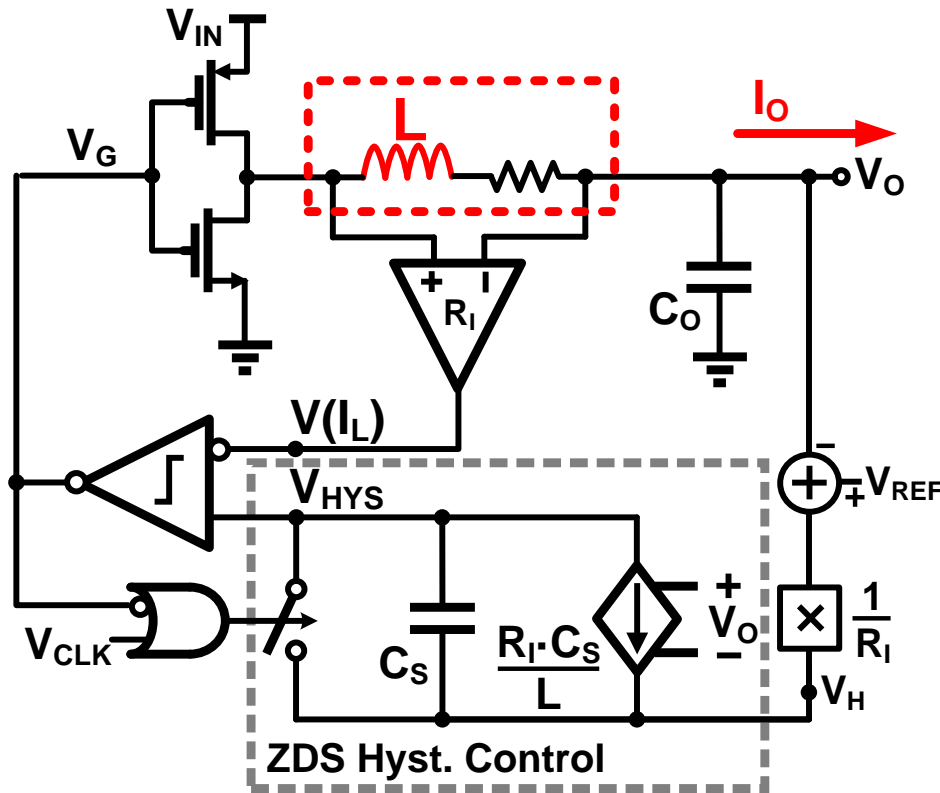
- Background and Challenges
- **Proposed Design**
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Limitations of Single-phase Implementation



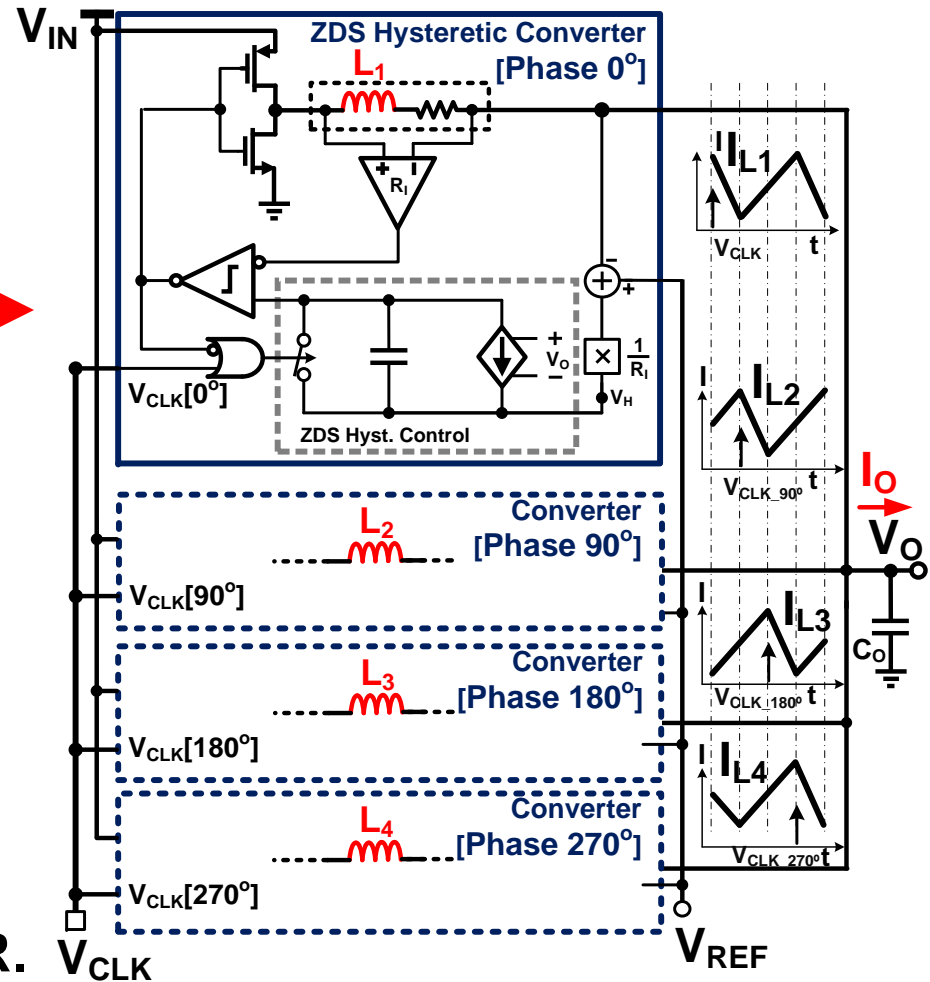
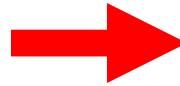
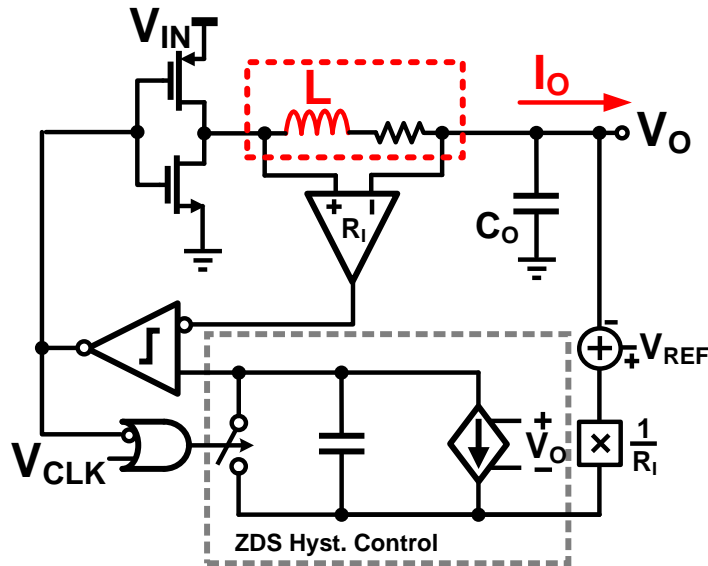
- Even with the fast zero-delay response..
 - I_L slew rate limited by the physical inductor size.

Limitations of Single-phase Implementation



- Even with the fast zero-delay response..
 - I_L slew rate limited by the physical inductor size.
 - Limited I_O slew rate – V_{DROOP}
 - Limited output power level – Efficiency and V_{DROOP}

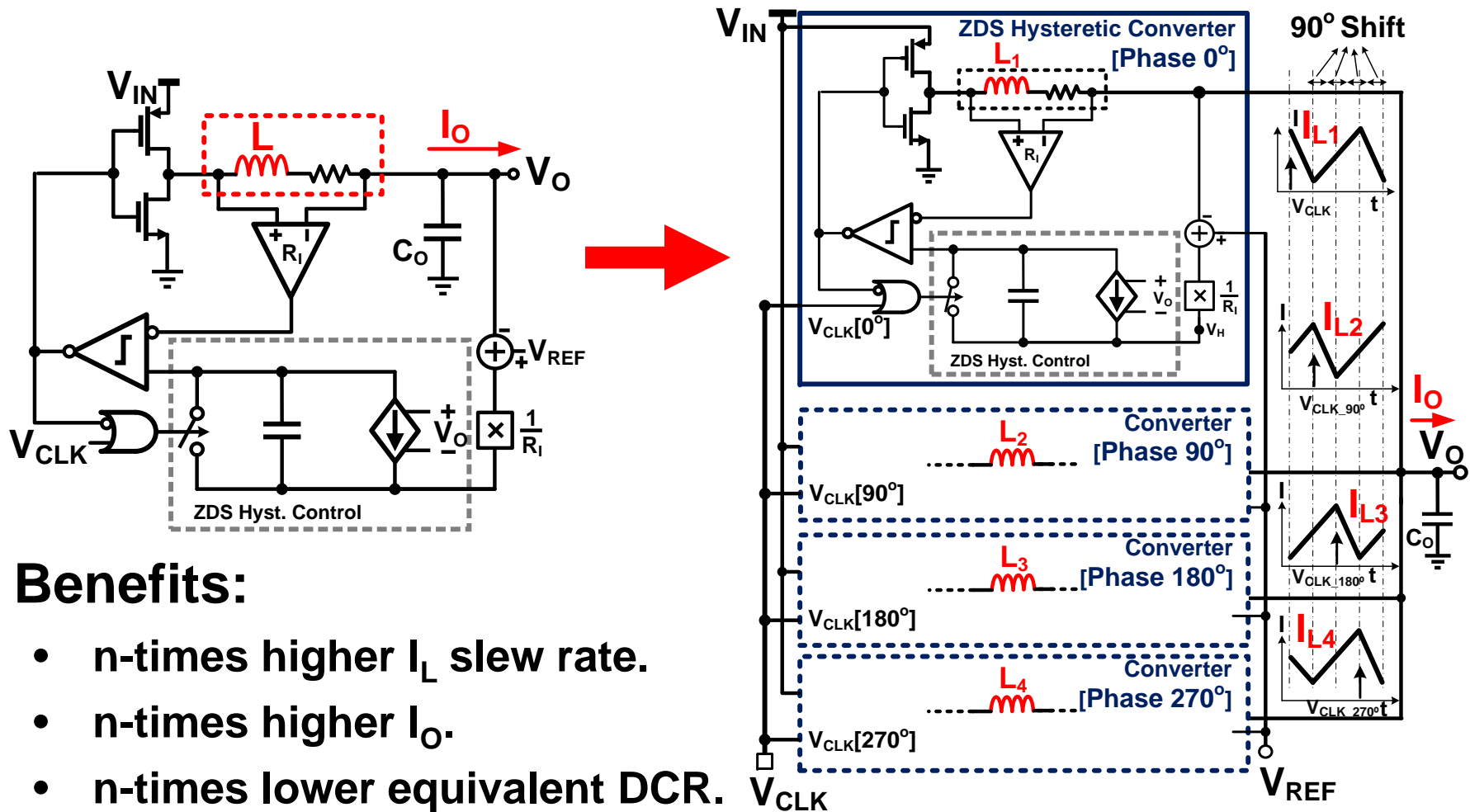
Solution: Multiphase Implementation



• Benefits:

- n-times higher I_L slew rate.
- n-times higher I_O .
- n-times lower equivalent DCR.

Solution: Multiphase Implementation



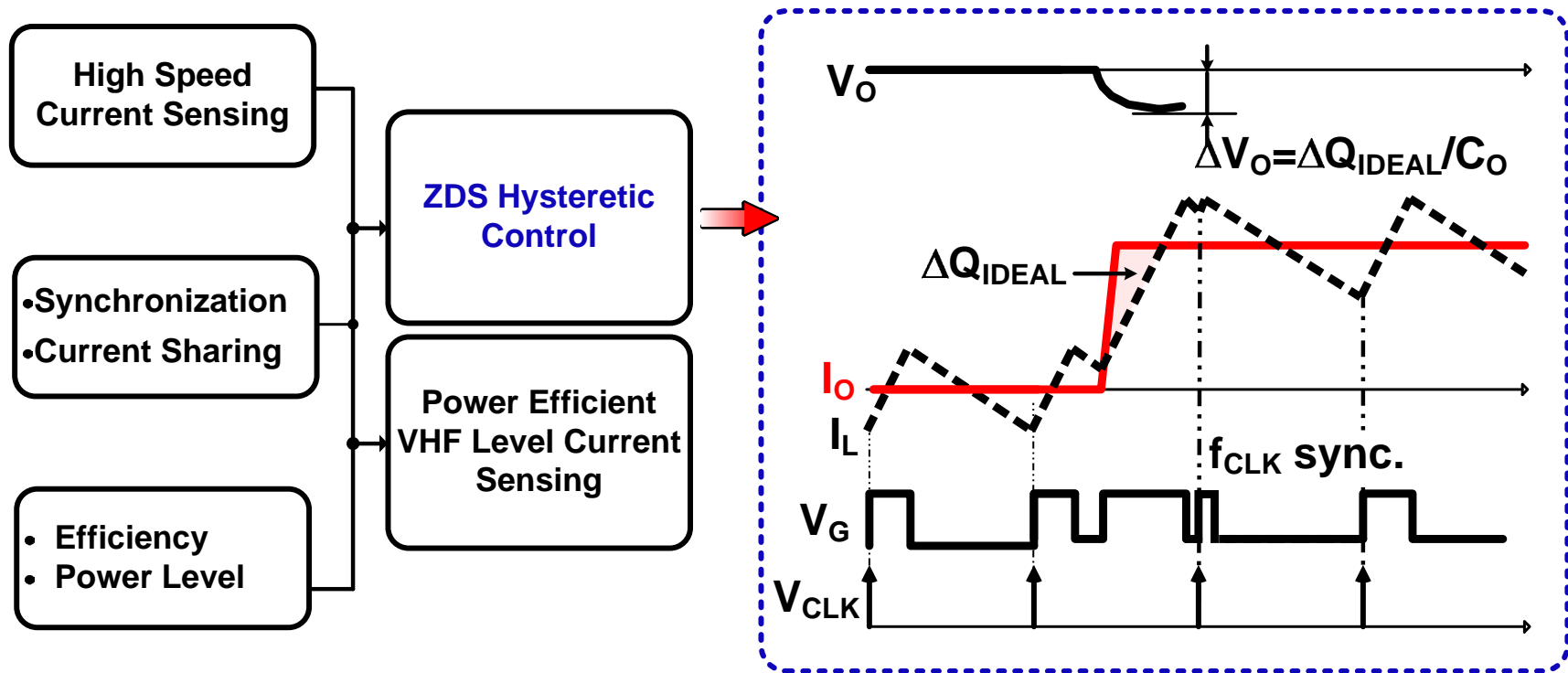
• Benefits:

- n-times higher I_L slew rate.
- n-times higher I_O .
- n-times lower equivalent DCR.

• Major Challenges:

- Clock and phase synchronization and current sharing.

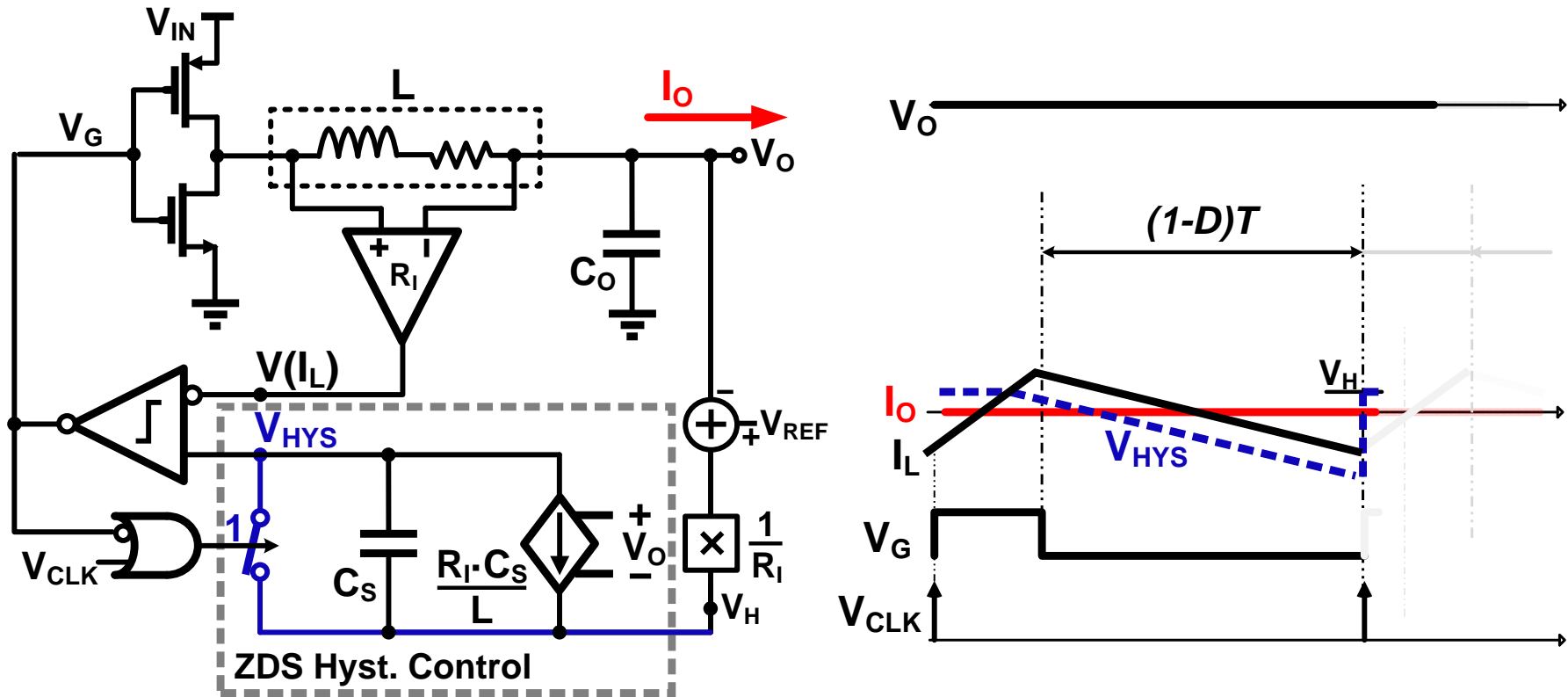
Key Features of ZDS Hysteretic Control



• Zero-Delay Synchronized Hysteretic Control

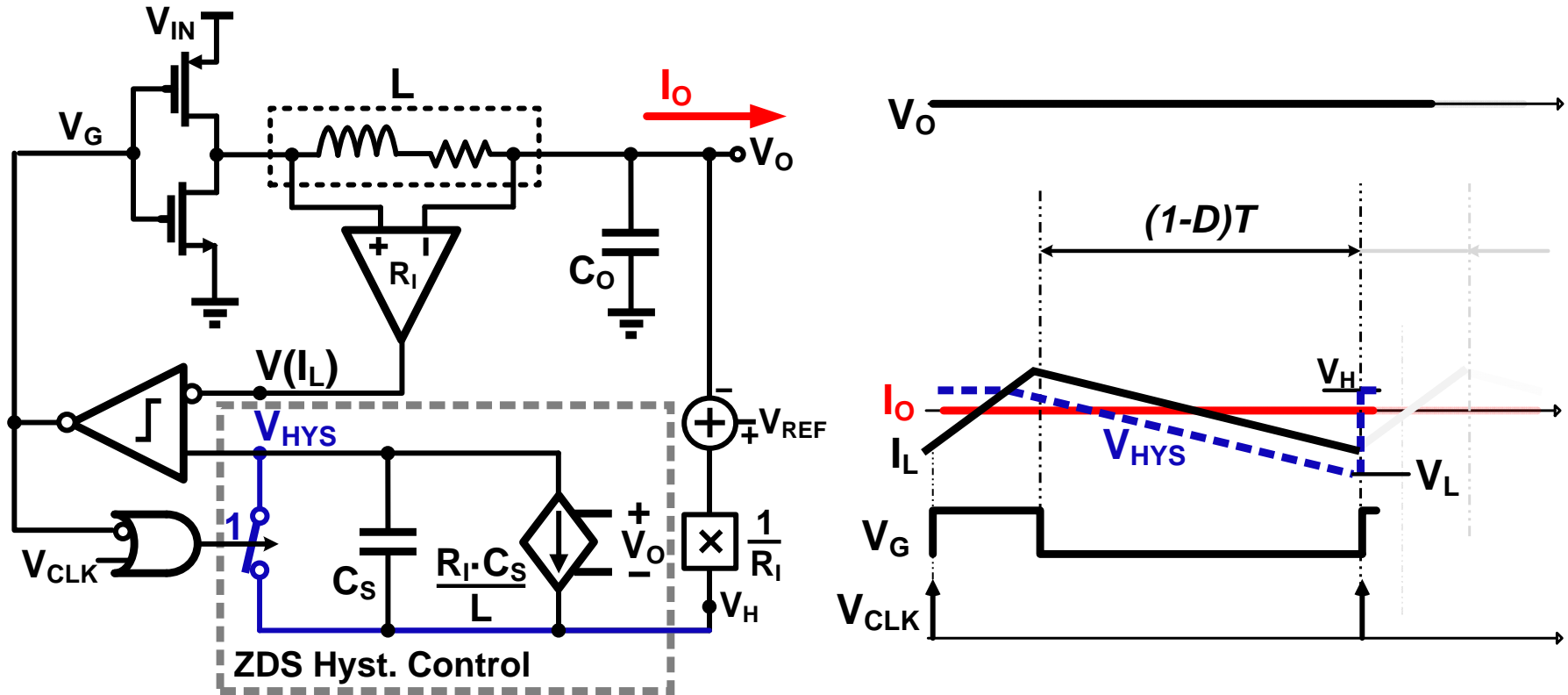
- *Synchronized f_{SW} for multiphase implementation.*
- *Current mode based operation for cycle-by-cycle current sharing.*

Control Scheme : f_{sw} Synchronization



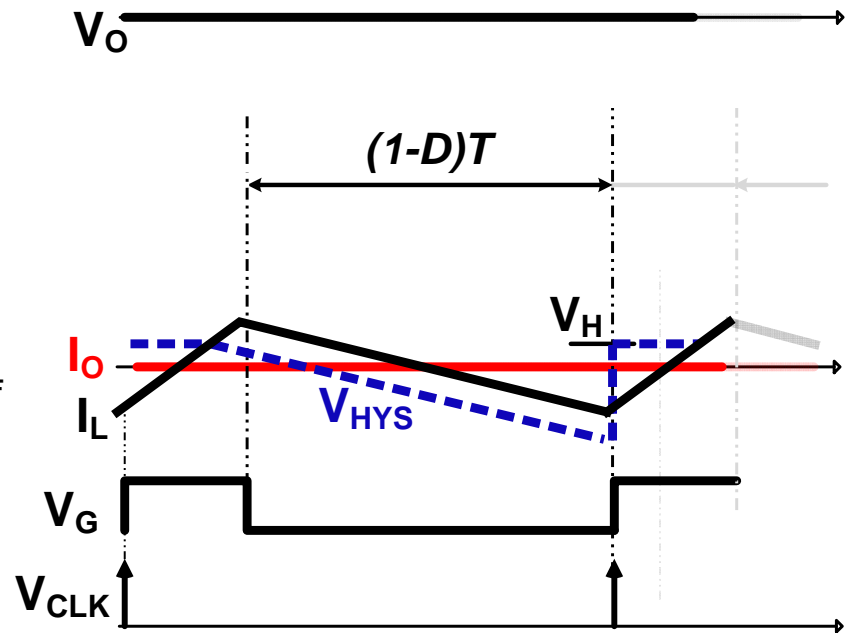
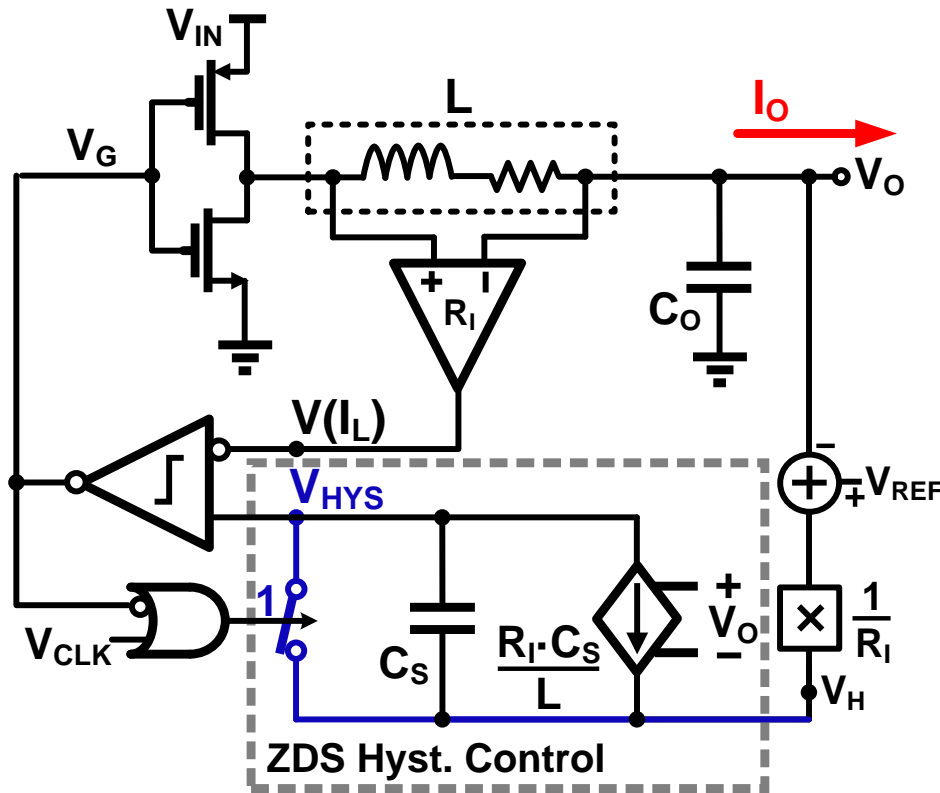
- At V_{CLK} pulse, V_{HYS} is reset to V_H .

Control Scheme : f_{sw} Synchronization



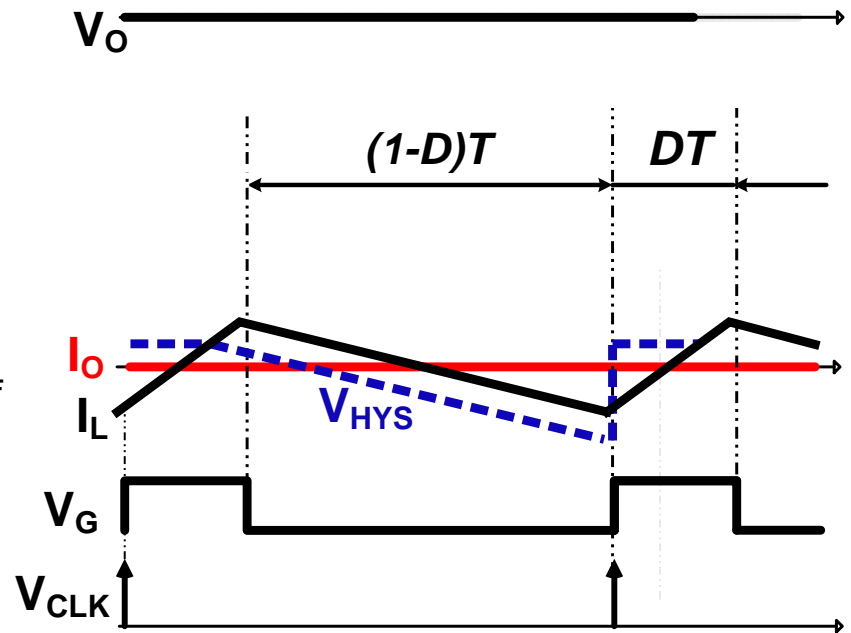
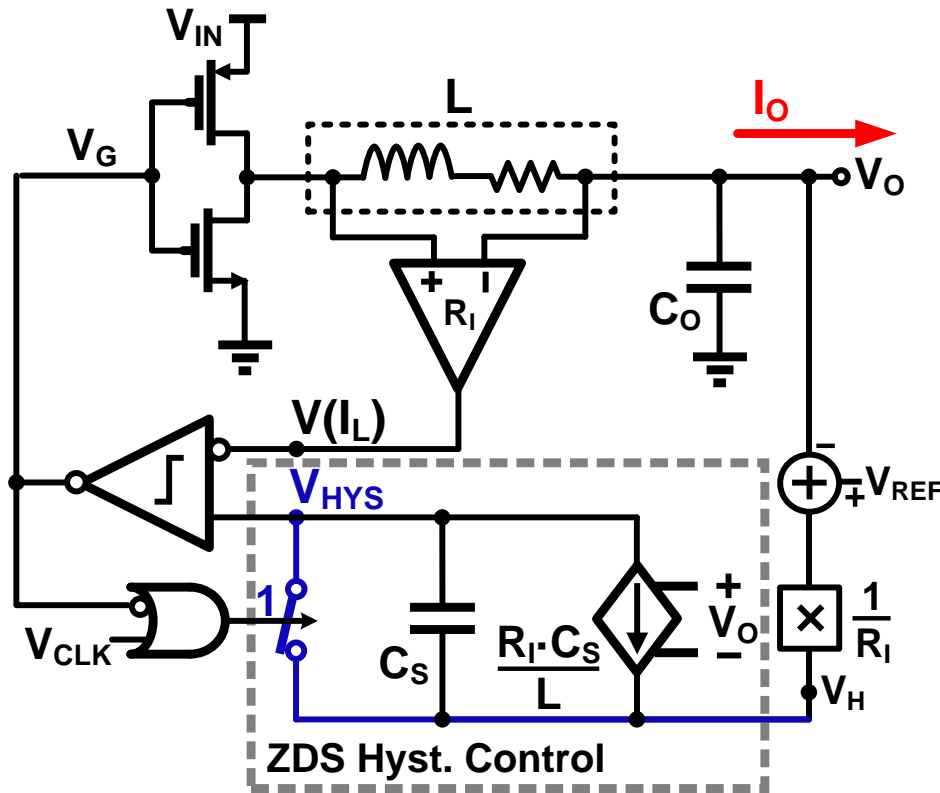
- At V_{CLK} pulse, V_{HYS} is reset to V_H .
- V_G turns on instantly when V_{HYS} hits I_L .
 - V_{HYS} acts like a lower hysteresis boundary, V_L .

Control Scheme : f_{sw} Synchronization



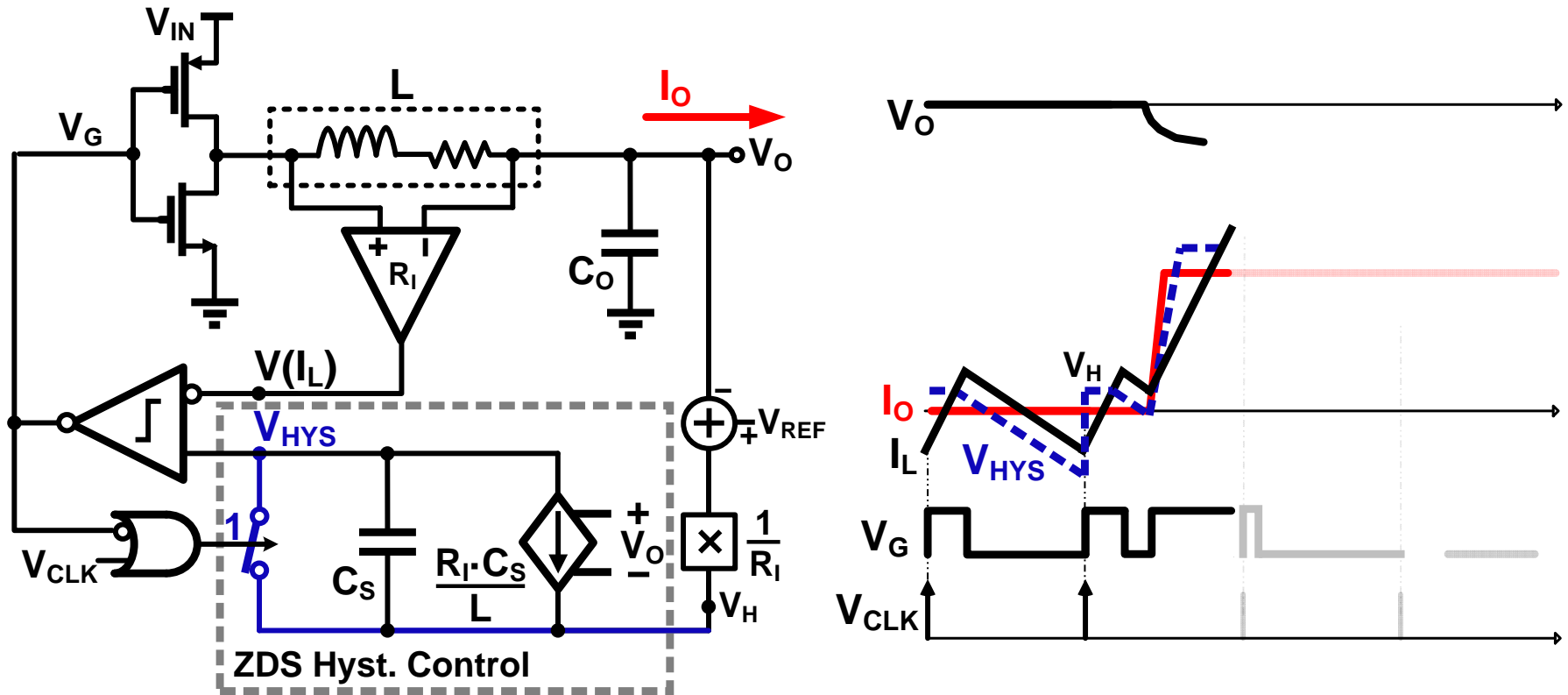
- At V_{CLK} pulse, V_{HYS} is reset to V_H .
- V_G turns on instantly when V_{HYS} hits I_L
- V_G remains on until I_L reaches to V_{HYS} .
 - V_{HYS} acts like an upper hysteresis boundary, V_H .

Control Scheme : f_{sw} Synchronization



- At V_{CLK} pulse, V_{HYS} is reset to V_H .
- V_G turns on instantly when V_{HYS} hits I_L
- V_G remains on until I_L reaches to V_{HYS} .
- The leading edge of DT is now synchronized to V_{CLK} .

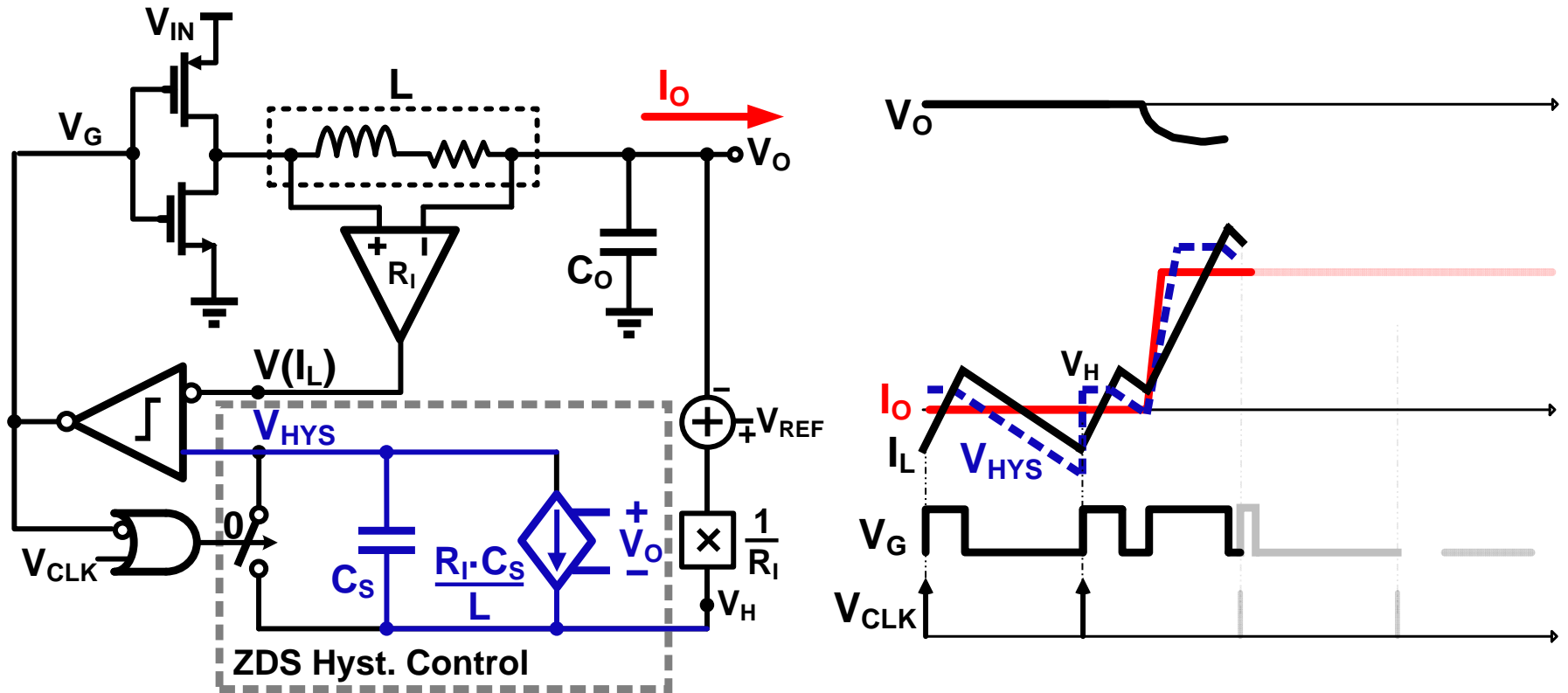
Loss of Synchronization When I_o Steps Up



• Loss of Synchronization

- V_G turns on immediately following I_o change without waiting for the next V_{CLK} pulse.
- The zero-delay response has priority over synchronization to V_{CLK} .

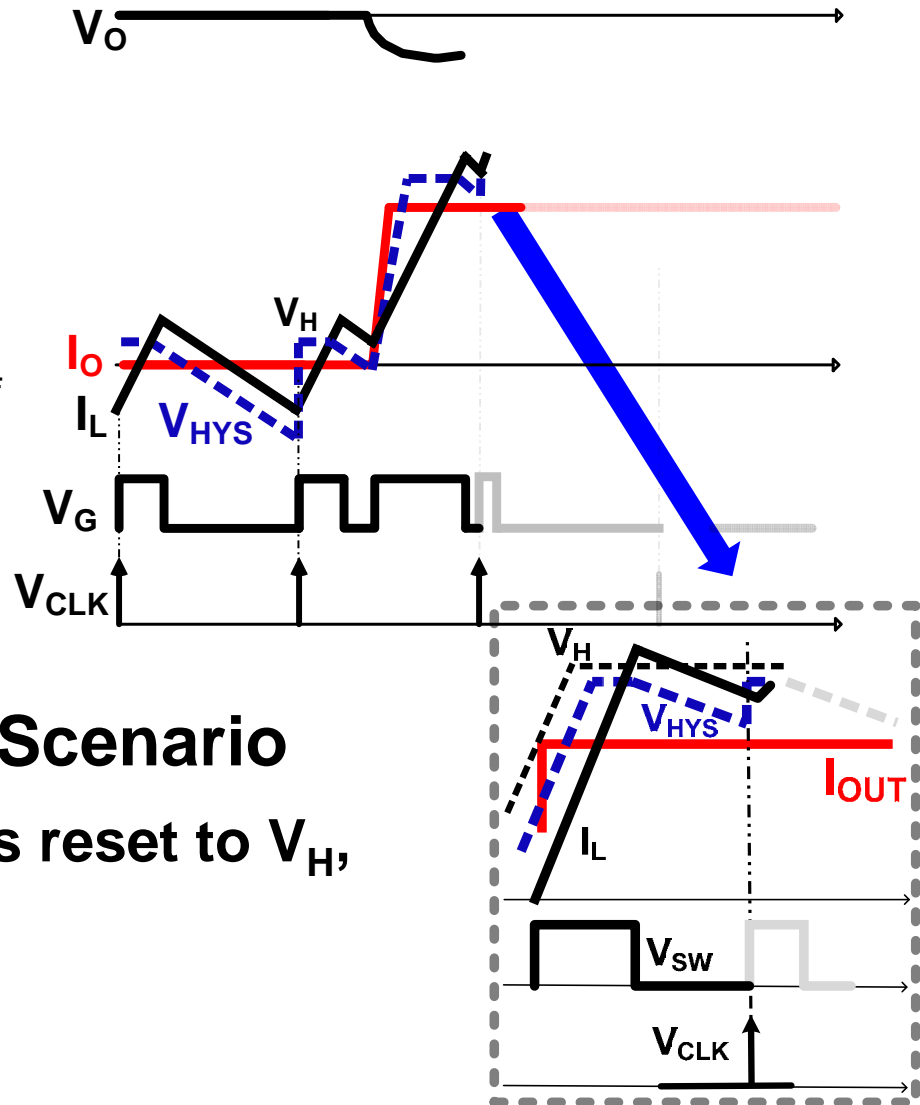
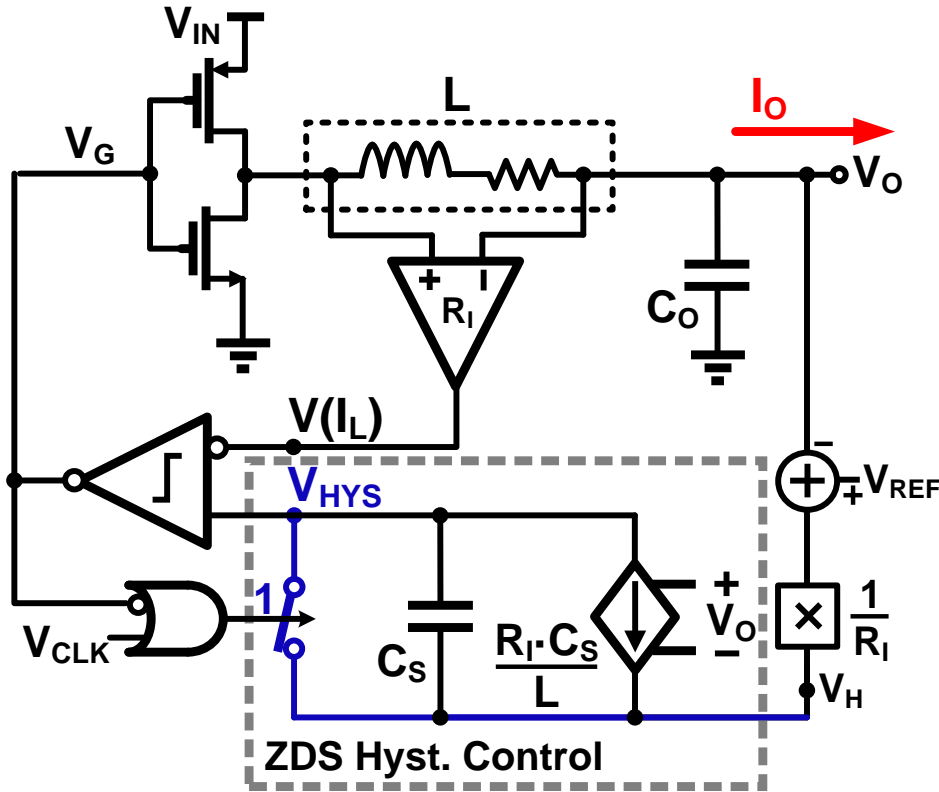
f_{sw} Synchronization Recovery



• Synchronization Recovery Scenario

- When I_L reaches V_H (*high I_O*), V_{HYS} again slides down from V_H .

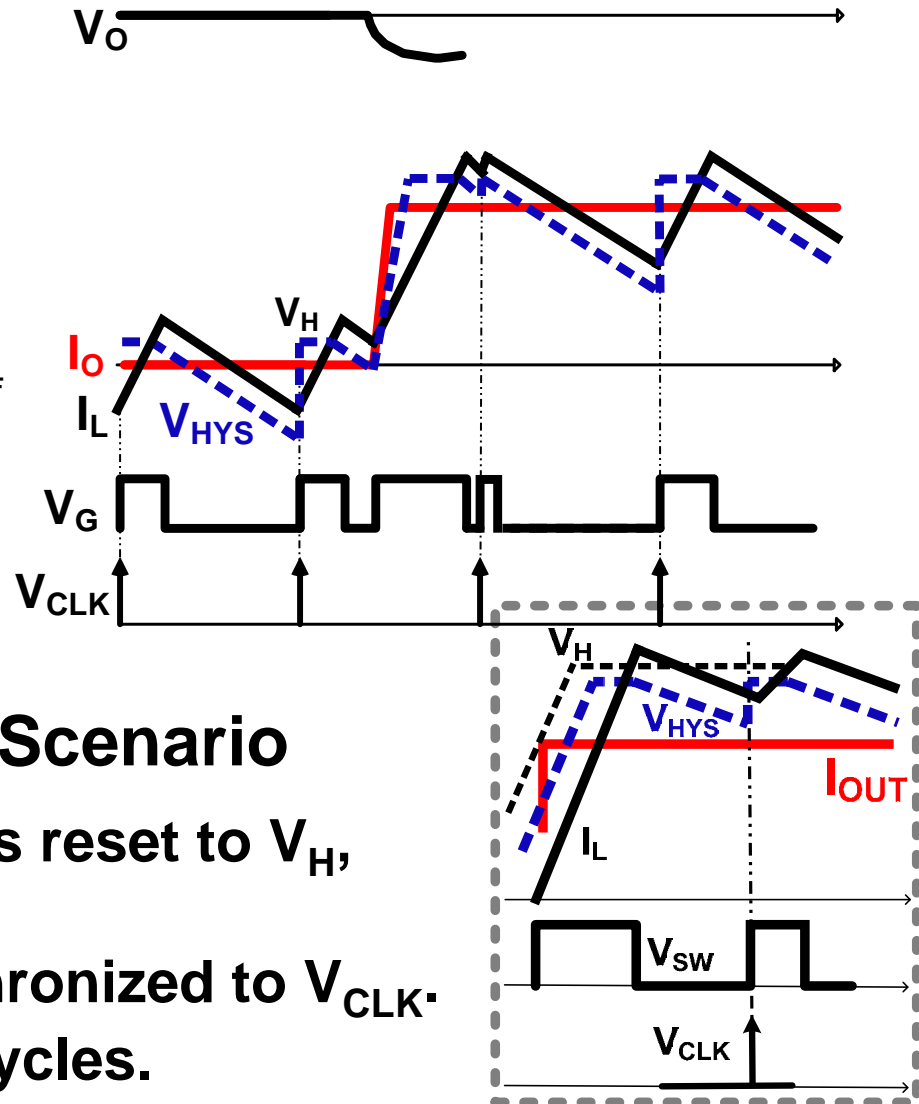
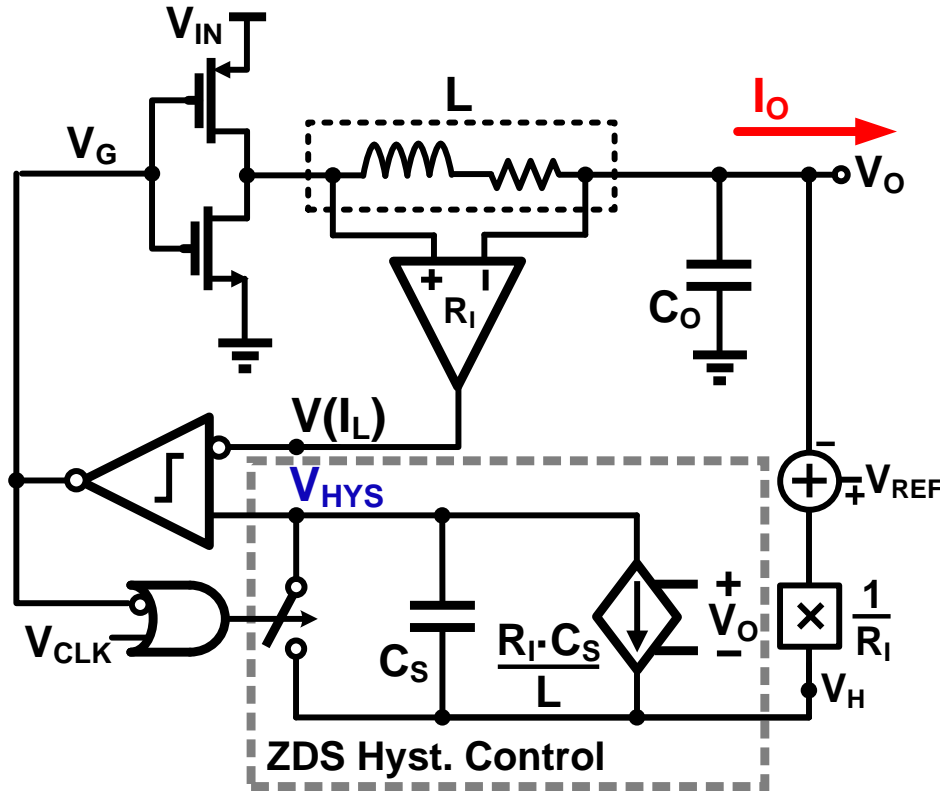
f_{sw} Synchronization Recovery



- **Synchronization Recovery Scenario**

- At the next V_{CLK} pulse, V_{HYS} is reset to V_H , triggering V_G on.

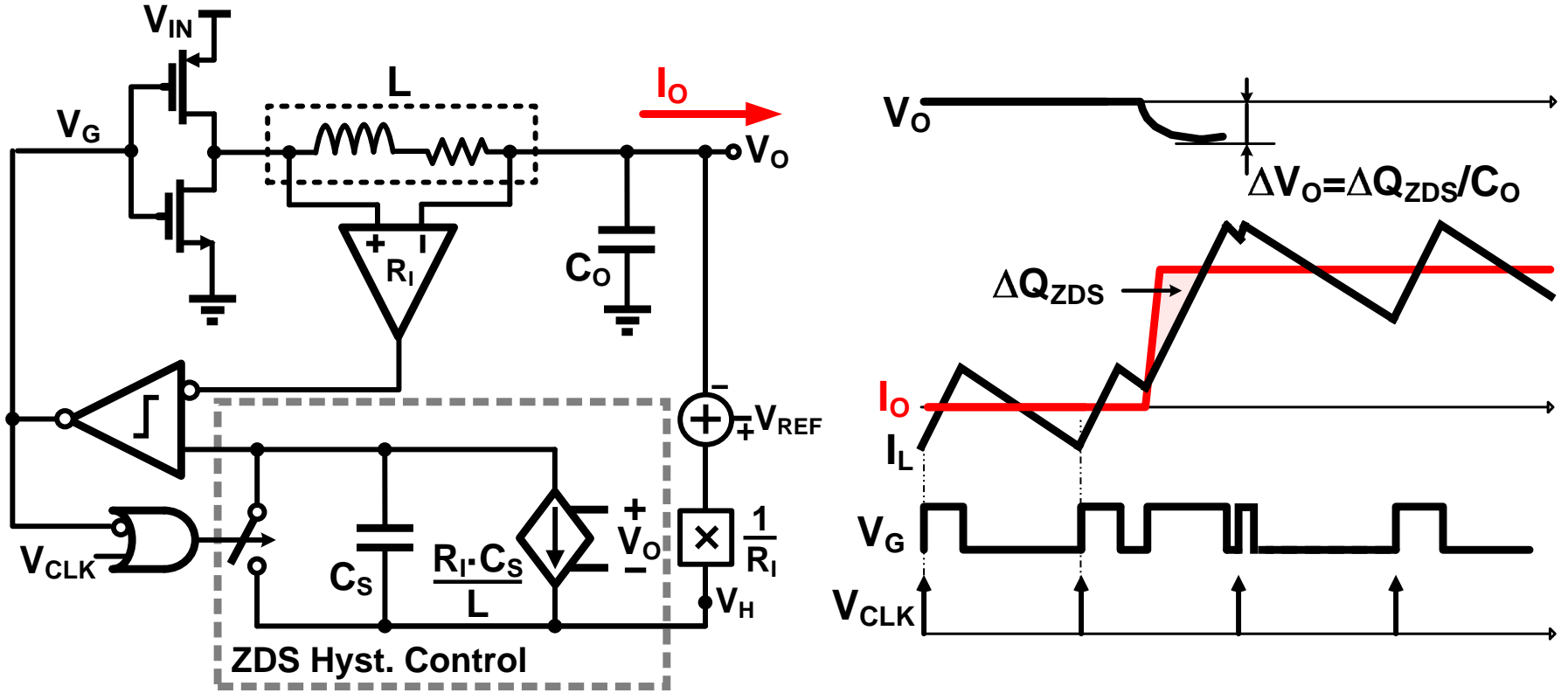
f_{sw} Synchronization Recovery



• Synchronization Recovery Scenario

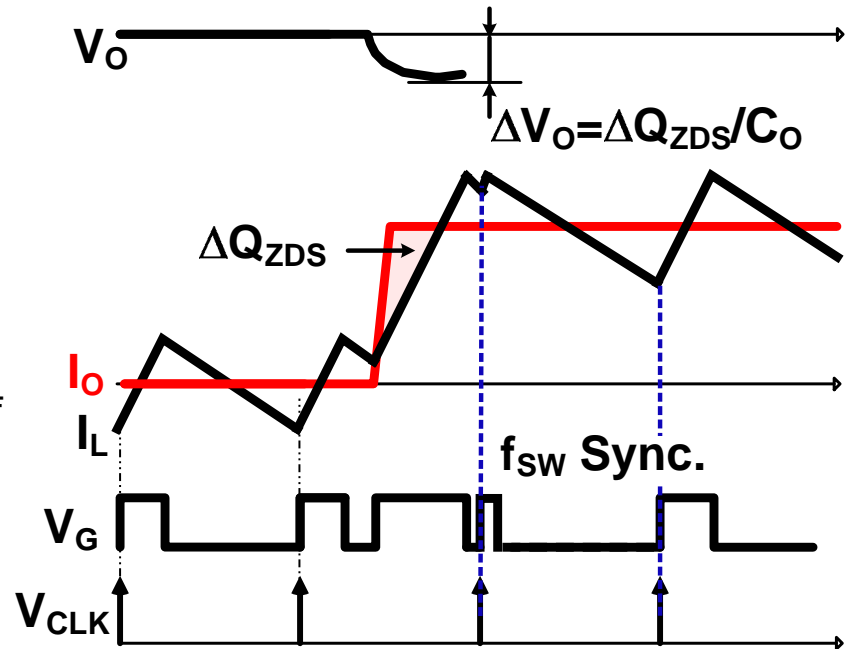
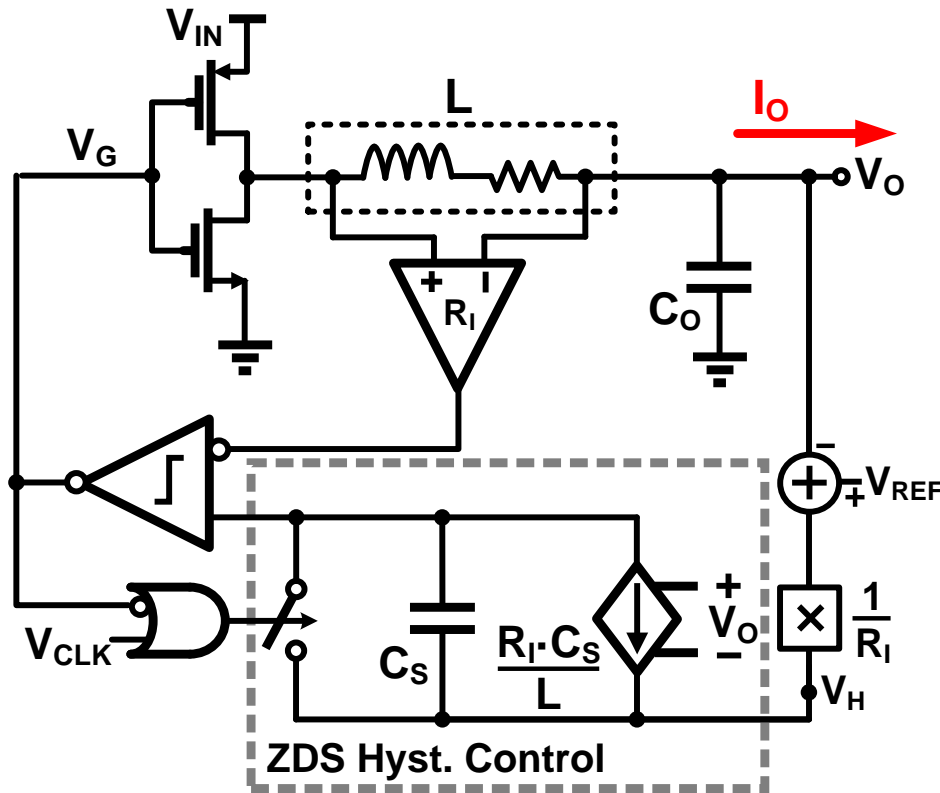
- At the next V_{CLK} pulse, V_{HYS} is reset to V_H , triggering V_G on.
- Leading edge of V_G is synchronized to V_{CLK} .
- I_L is stabilized within a few cycles.

Control Scheme: Summary



- **Near Zero Delay Hysteretic Response:**
 - $\Delta Q_{ZDS} < \Delta Q_{HYSTERETIC} \ll \Delta Q_{PWM}$

Control Scheme: Summary



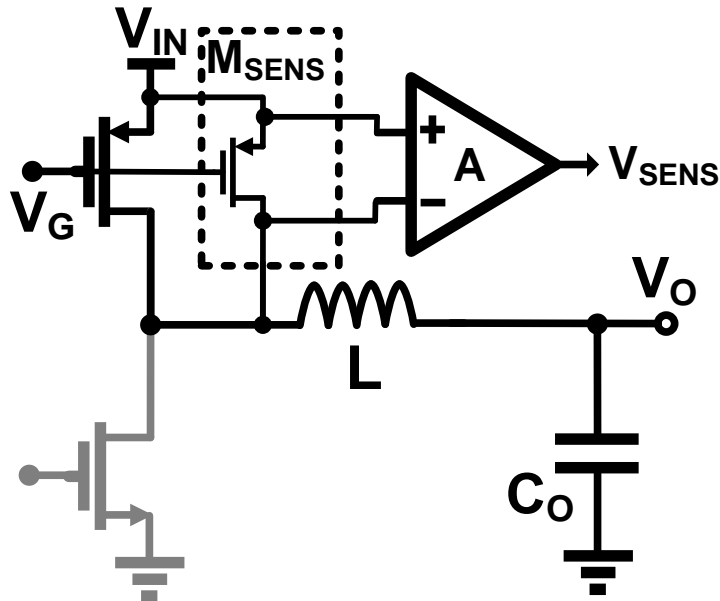
- **Near Zero Delay Hysteretic Response:**
 - $\Delta Q_{ZDS} < \Delta Q_{HYSTERETIC} \ll \Delta Q_{PWM}$
- **Multiphase Implementation:**
 - *Clock and phase synchronization, cycle-by-cycle current sharing.*

Outline

- Background and Challenges
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 - Wide Range Efficiency
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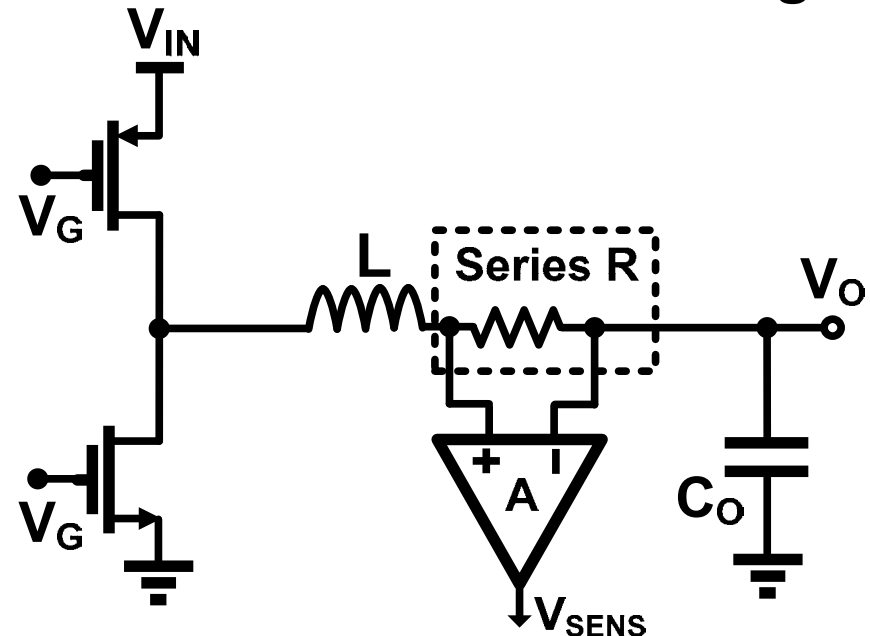
I_L -Sensing Limitations on VHF Operation

Transistor R_{DS} Sensing



- L_X -spiking.
- Discontinuous.
- Wide-bandwidth amplifier required.

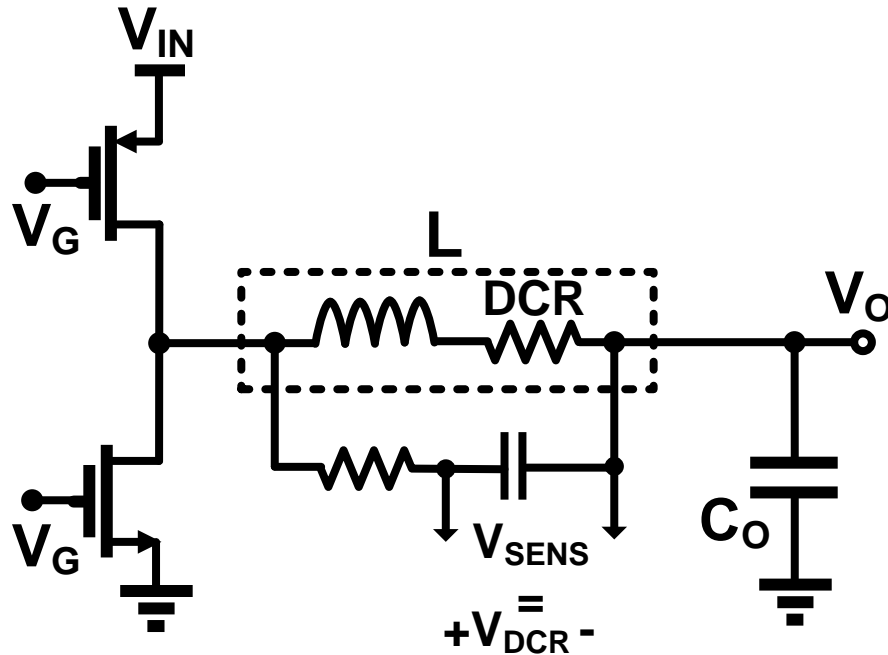
Series R_{SENS} Sensing



- Continuous.
- Power loss.
- Wide-bandwidth amplifier required.

I_L -Sensing Limitations on VHF Operation

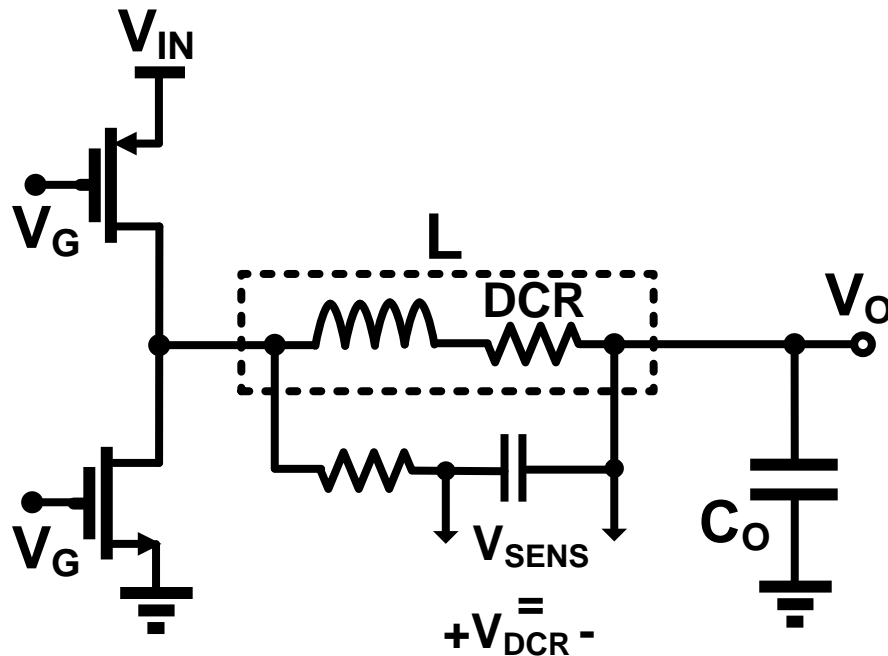
Inductor DCR Sensing



- **Pros:**
 - Continuous I_L sensing.
 - No additional power loss from series R.

I_L -Sensing Limitations on VHF Operation

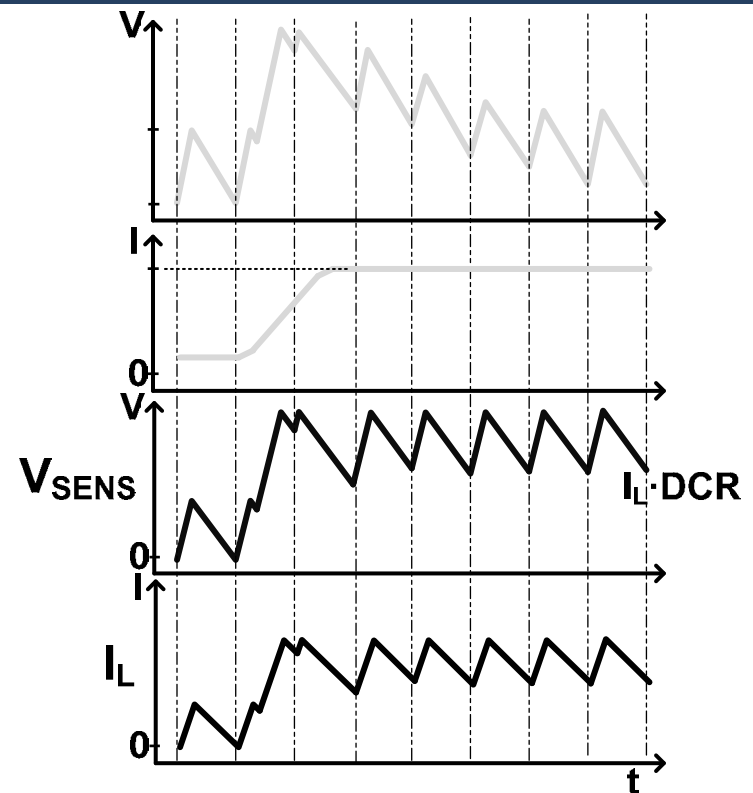
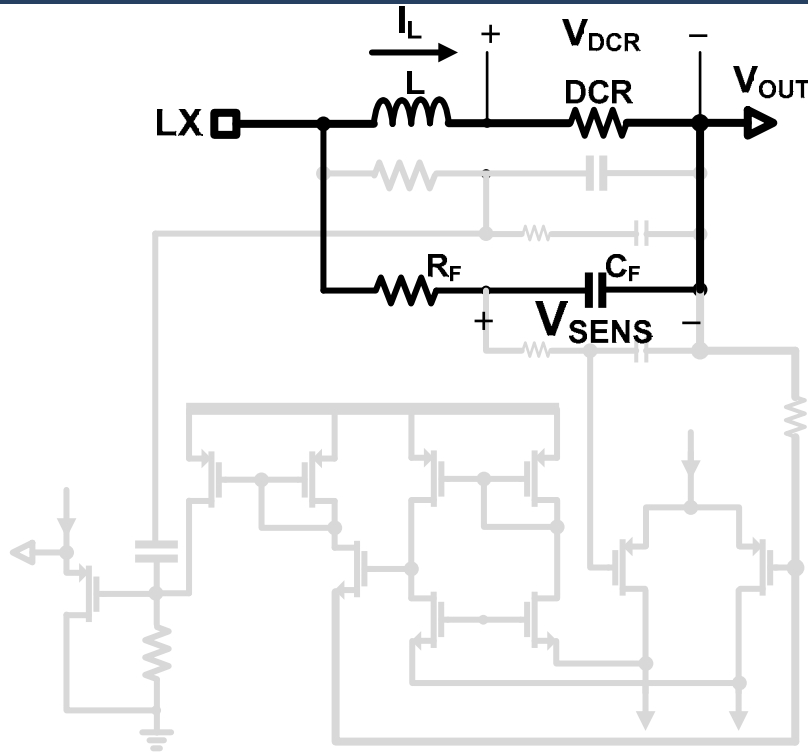
Inductor DCR Sensing



- **Pros:**
 - Continuous I_L sensing.
 - No additional power loss from series R.
- **Cons:**
 - Small DCR.
 - Insufficient current sense gain requires additional wide-bandwidth amplifier.

More power consumption as f_{sw} increases!

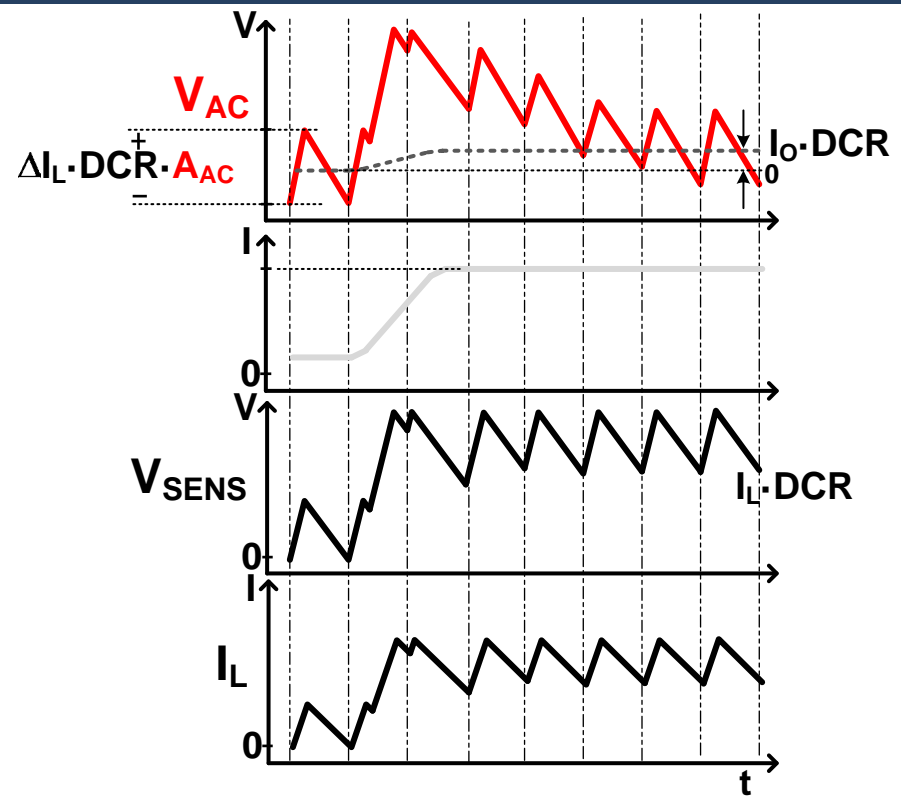
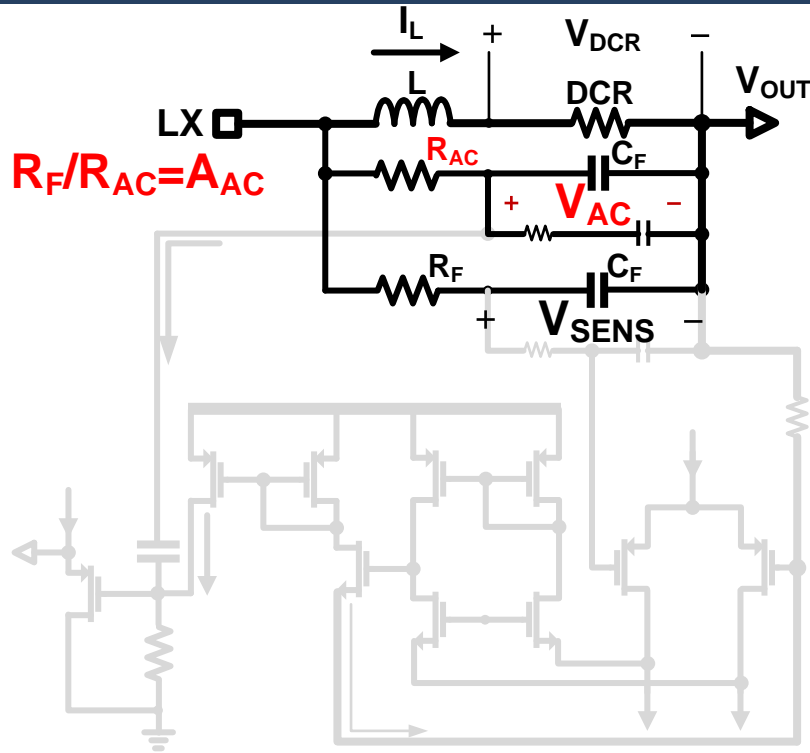
Emulated AC+DC Current Sensor



- **New Idea of Current Sensing**

- Split the AC (fast) and DC (slow) portion of I_L , amplify them separately, and combine them together.
- It eliminates the need for a power hungry wide-bandwidth amplifier in order to amplify the V_{DCRs} .

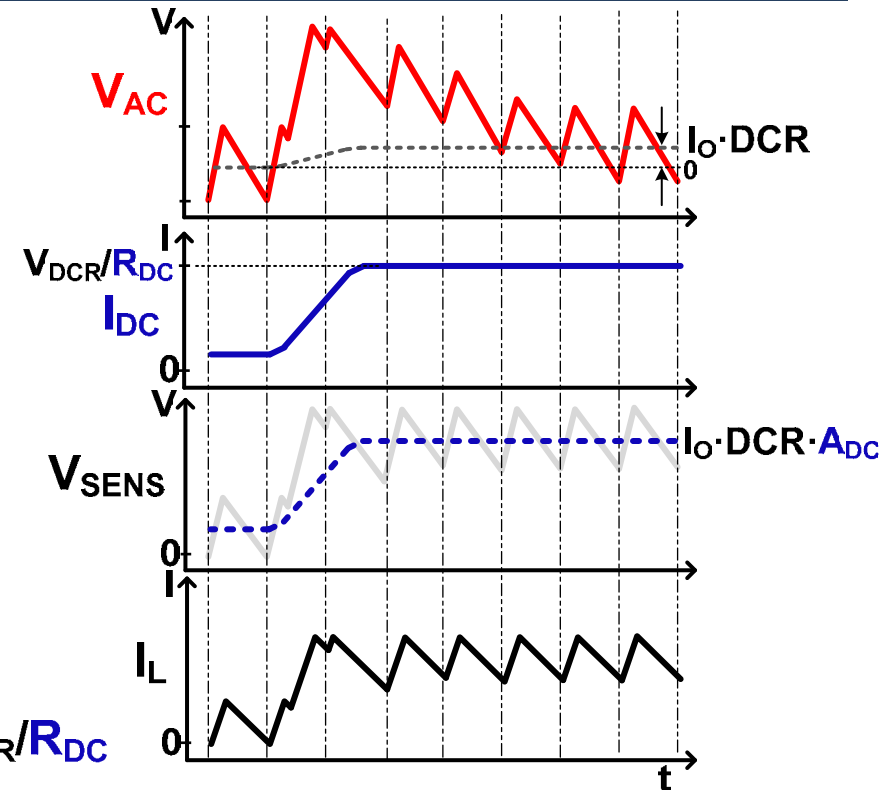
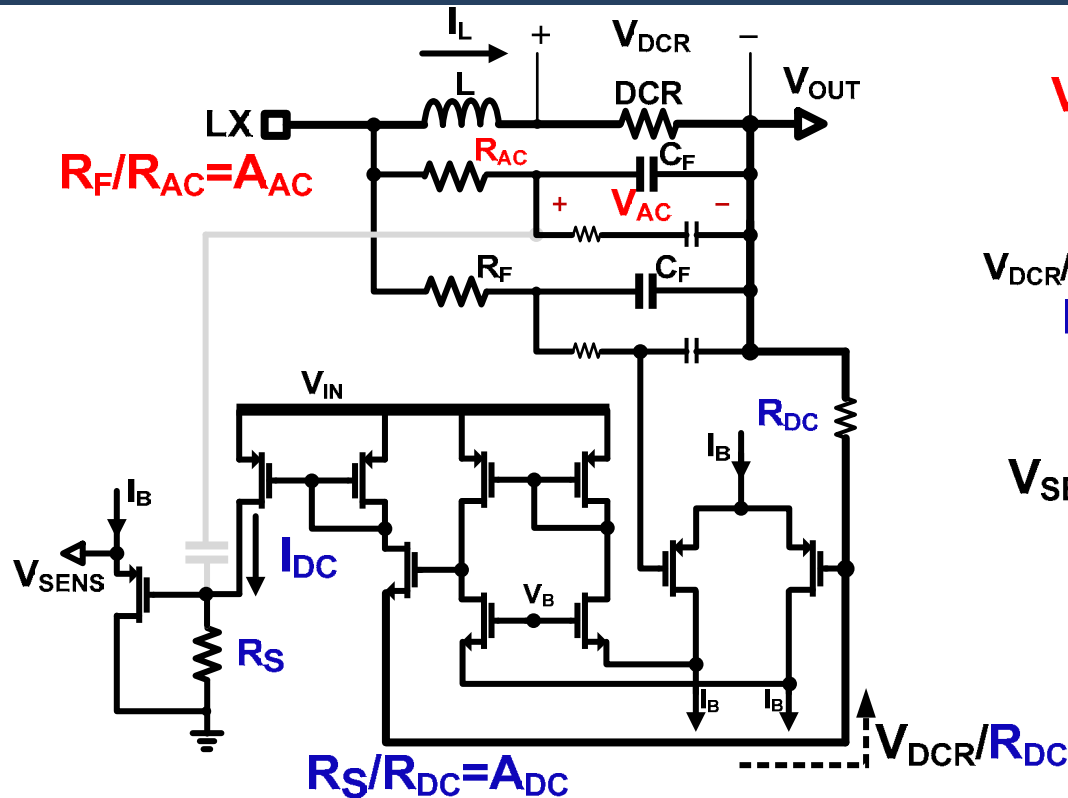
Emulated AC+DC Current Sensor



• AC Amplification

- Fast portion of I_L is amplified without power consumption.
- ΔI_L is emulated using smaller RC filter = $\Delta V_{AC}/\Delta V_{SENS} = A_{AC}$.
- As for the current sense gain R_I , DCR is amplified by A_{AC} .
- V_{AC} still lacks the DC information of I_L .

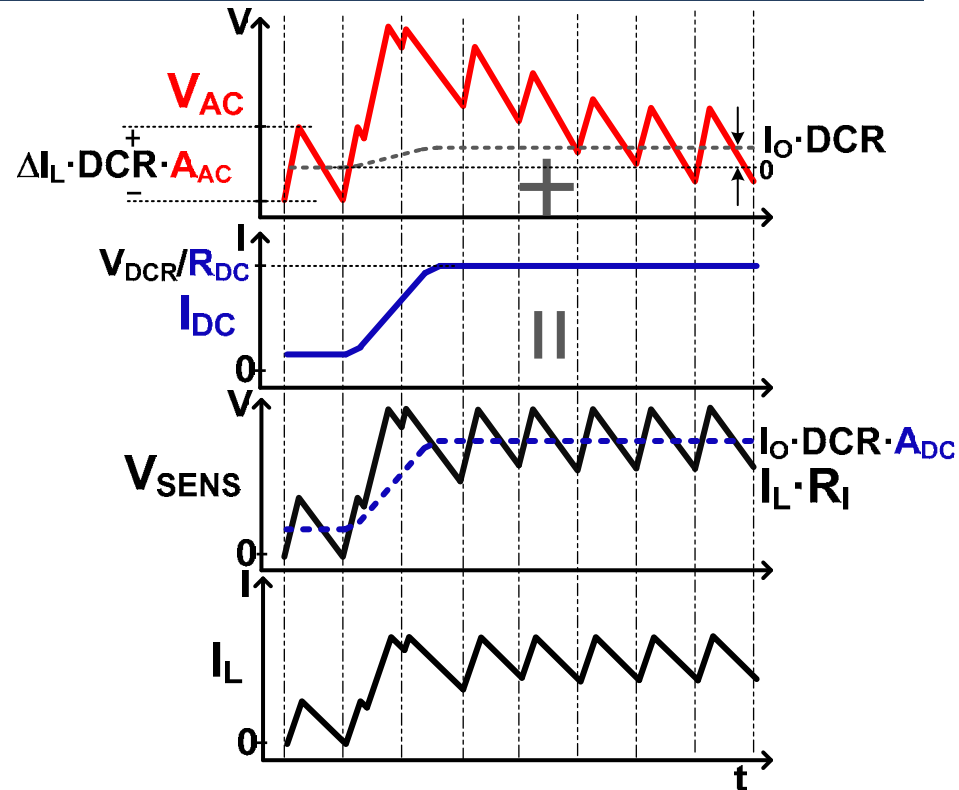
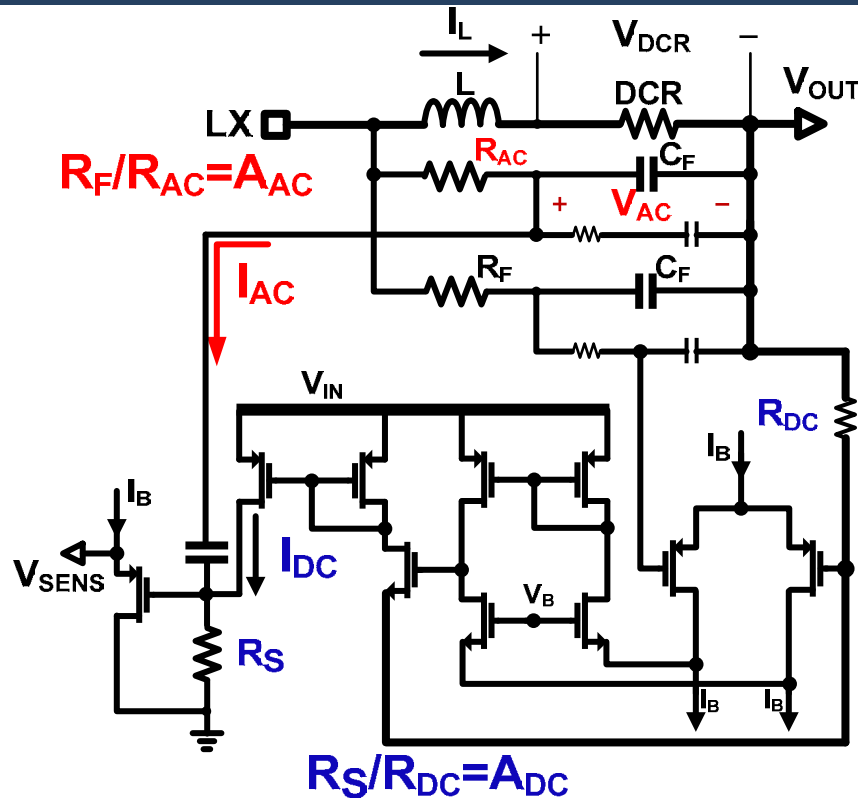
Emulated AC+DC Current Sensor



• DC Amplification

- Slow portion of I_L does not require a wide-bandwidth amplifier.
- Current conveyor senses the average of V_{DCR} and generates DC I_L emulated I_{DC} , as $I_{DC} = V_{DCR}/R_{DC}$.
- As for the current sense gain R_I , DCR is amplified by $R_S/R_{DC} = A_{DC}$.

Emulated AC+DC Current Sensor

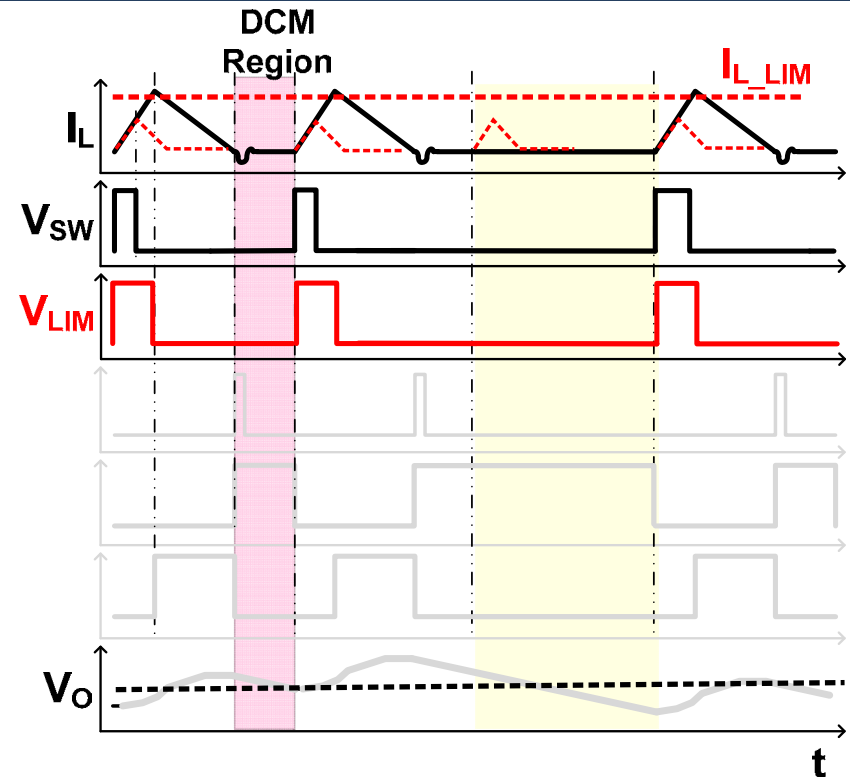
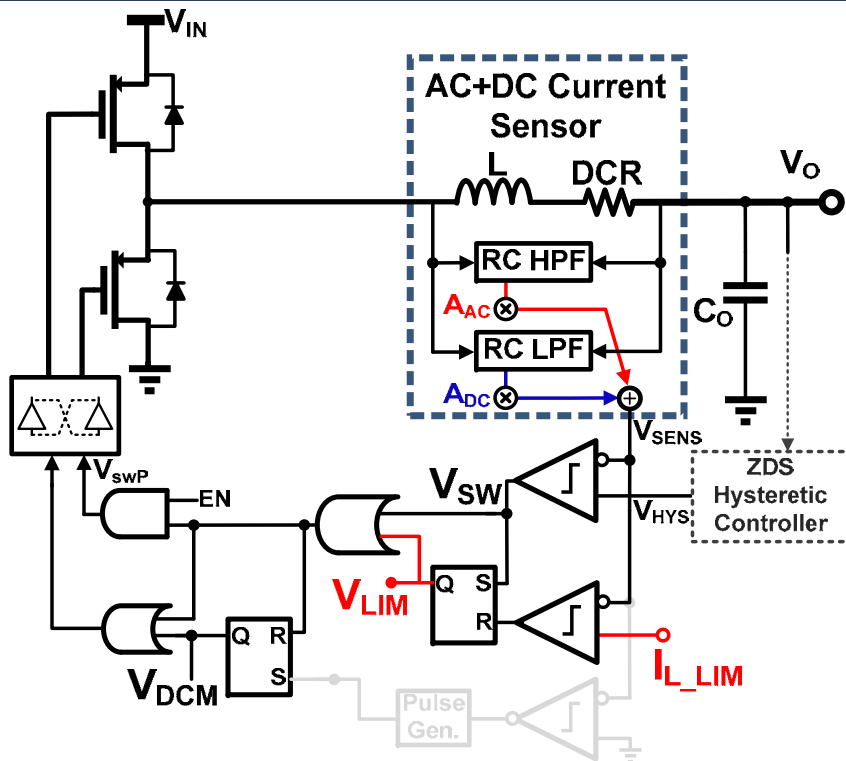


- Combining AC and DC Portions of Entire I_L
 - V_{AC} is coupled to output, V_{SENS} , through a capacitor.
 - By setting $A_{AC} = A_{DC} = A_{SENS}$, the overall current sense gain,
 $R_I = DCR \cdot A_{SENS}$.

Outline

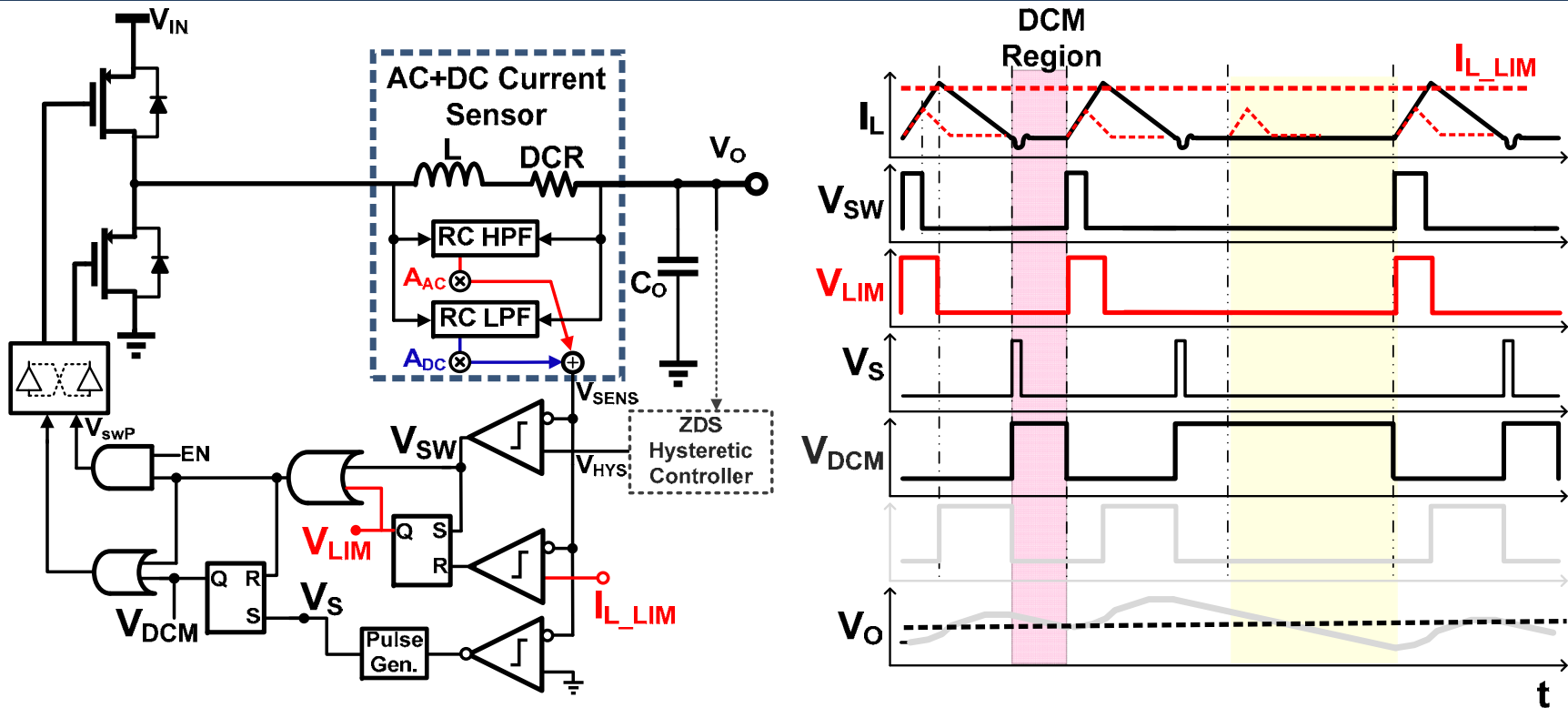
- Backgrounds and Challenges
- **Proposed Design**
 - Control Scheme : Zero Delay Response
 - Control Scheme : f_{sw} Synchronization
 - Emulated AC+DC Current Sensing
 - **Wide Range Efficiency**
- System Architecture
- Measurement Results
- Comparison and Conclusion

I_L -sensed DCM and Burst Mode Control



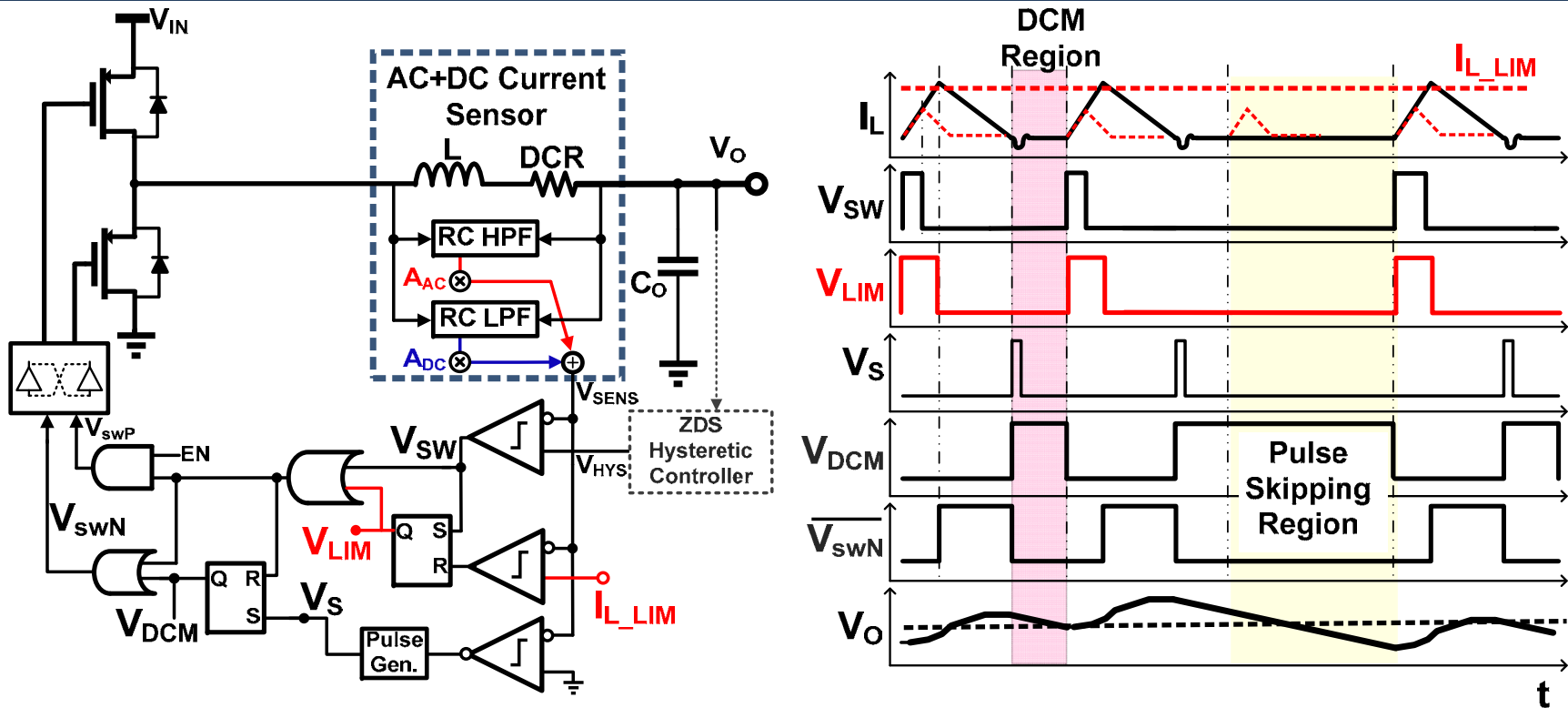
- For light load $< 200\text{mA}$, the controller saturates the duty ratio below the minimum duty ratio that is set by the **minimum peak I_L value**.

I_L -sensed DCM and Burst Mode Control



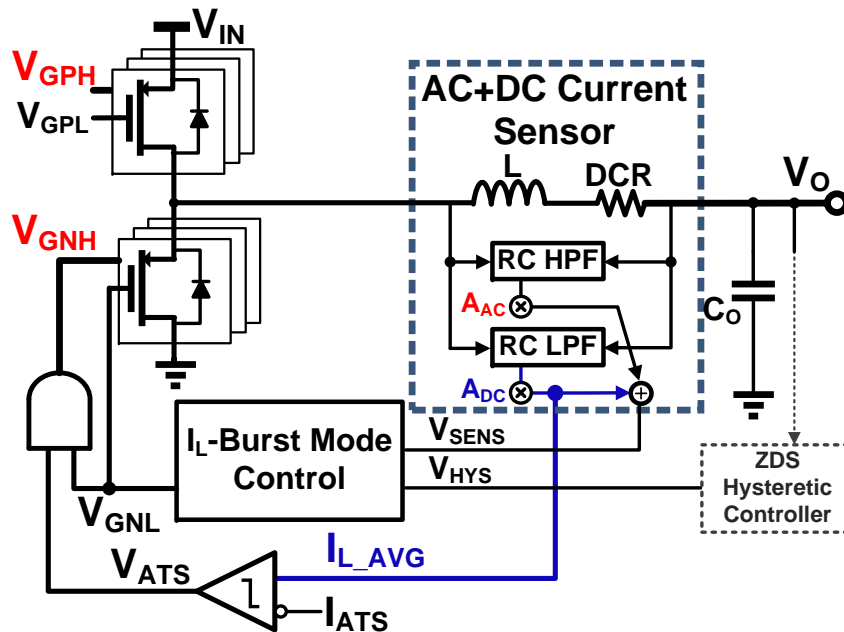
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- With the continuous I_L sensing feature of the AC+DC sensor, the controller stays in **DCM** never allowing I_L goes below zero.

I_L -sensed DCM and Burst Mode Control



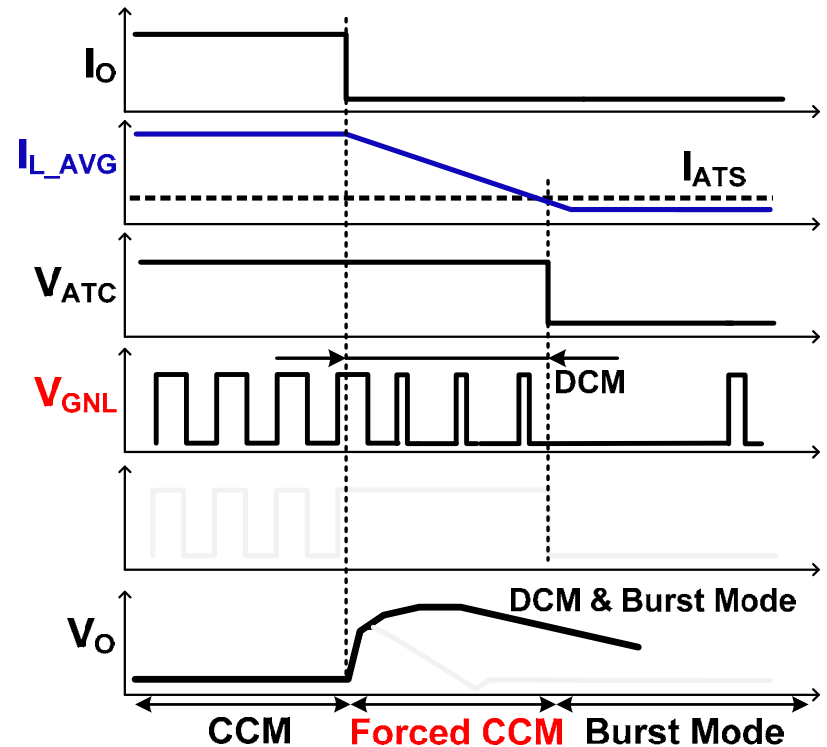
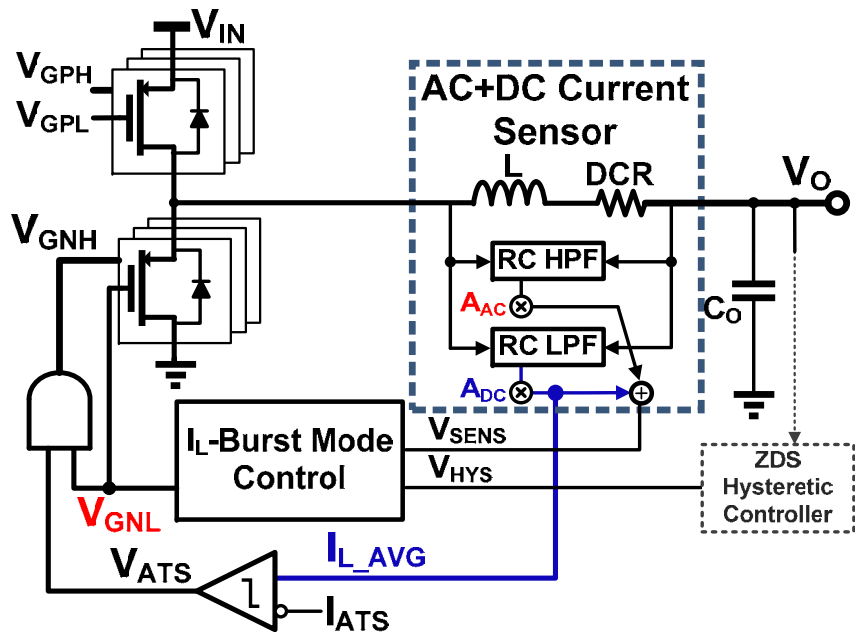
- For light load $< 200\text{mA}$, the controller saturates the duty ratio below the minimum duty ratio that is set by the **minimum peak I_L value**.
- With the continuous I_L sensing feature of the AC+DC sensor, the controller stays in **DCM** never allowing I_L goes below zero.
- As I_o goes lower, pulse skipping will occur as V_o ripple increases.

ATS and Forced-CCM



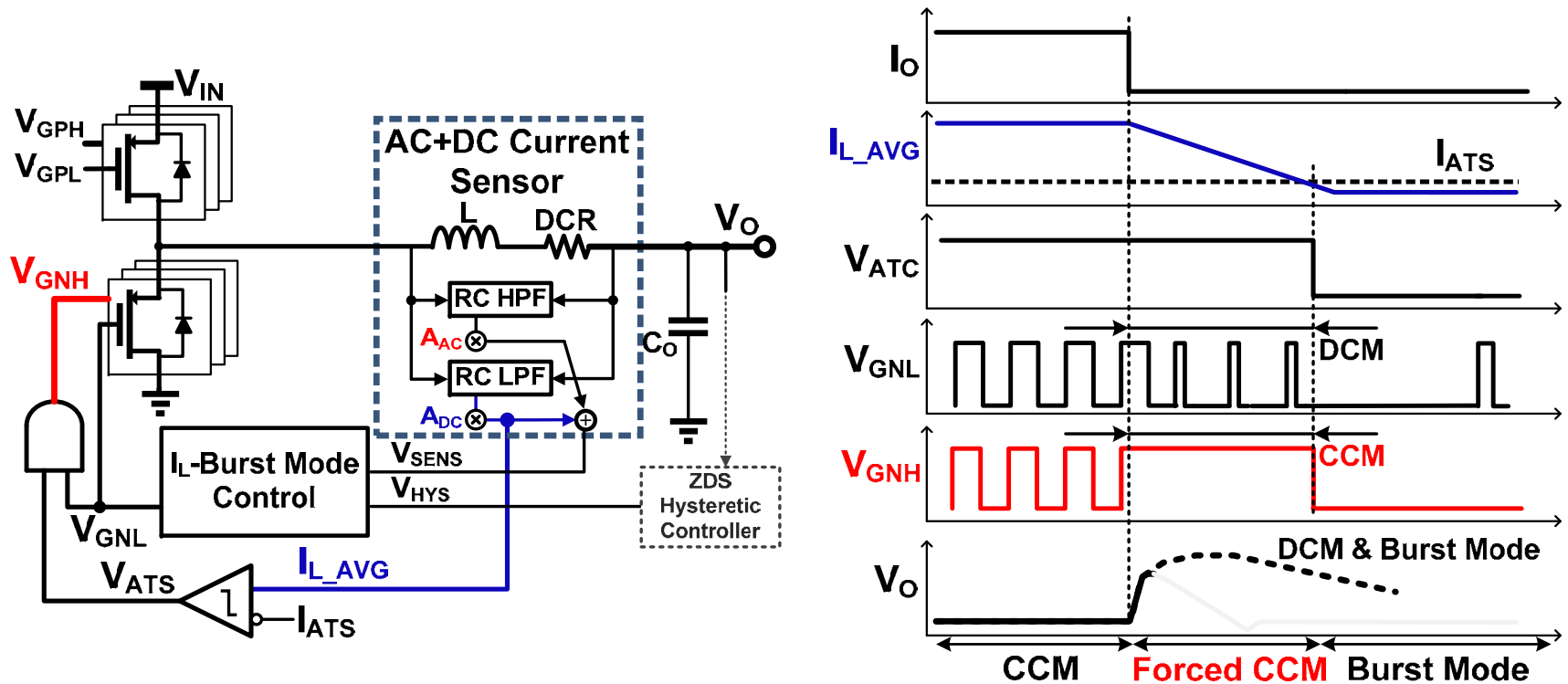
- For heavy load $>1.5A$, the **adaptive transistor sizing** (ATS) is performed only using DC I_L (I_{L_AVG}) without additional I_O sensing circuits.
- The divided power transistor stages will turn on/off depending on if I_{L_AVG} travels higher/lower than the ATS reference, I_{ATS} .

ATS and Forced-CCM



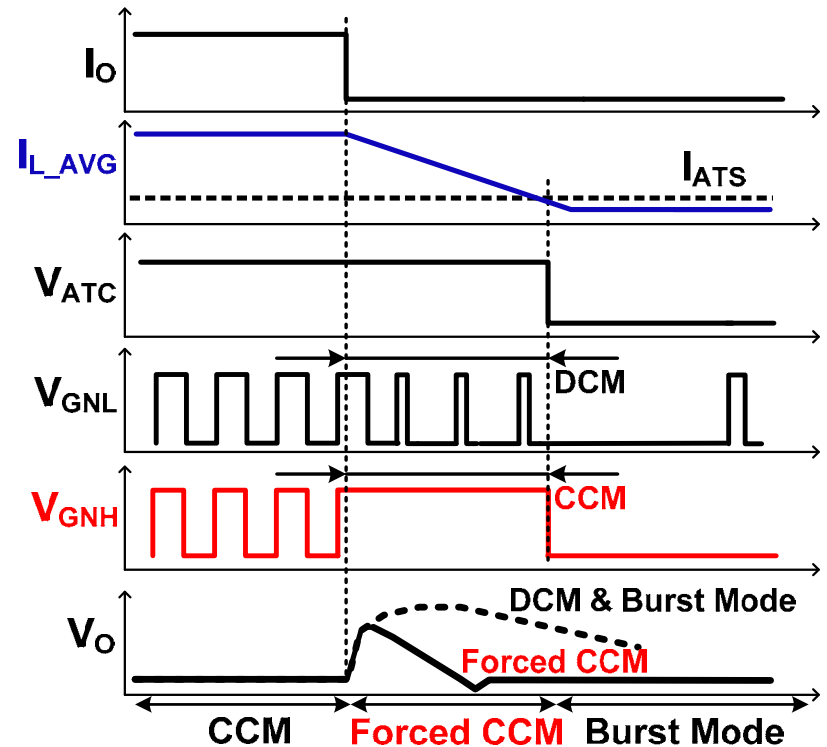
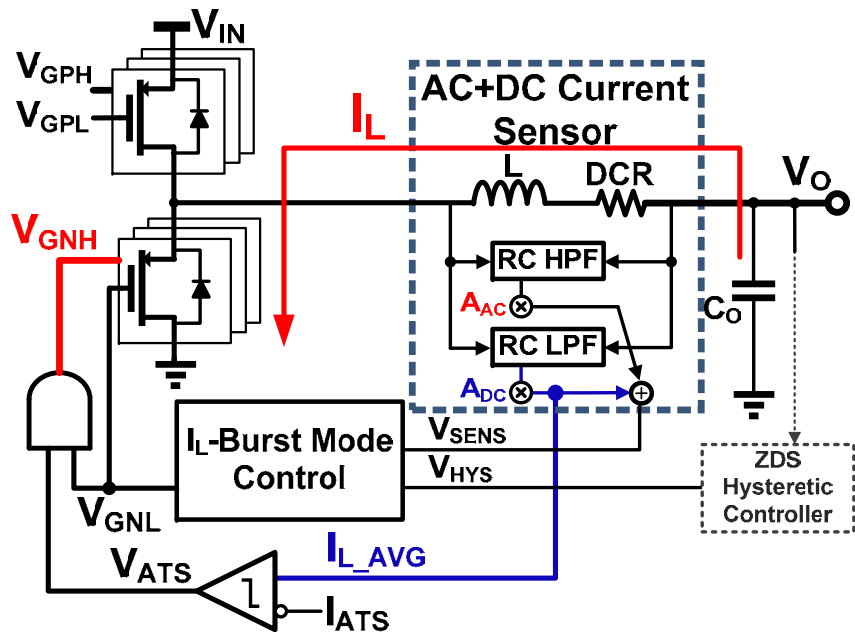
- When I_O steps down and large V_O overshoot occurs, ATS stage 1 (V_{GPL}, V_{GNL}) will immediately transition into burst mode control.

ATS and Forced-CCM



- When I_O steps down and large V_O overshoot occurs, ATS stage 1 (V_{GPL} , V_{GNL}) will immediately transition into burst mode control.
- Before ATS stages 2,3 (V_{GPH} , V_{GNH}) are completely shut off due to the I_O step-down, they momentarily remain in CCM until I_{L_AVG} hits I_{ATS} .

ATS and Forced-CCM

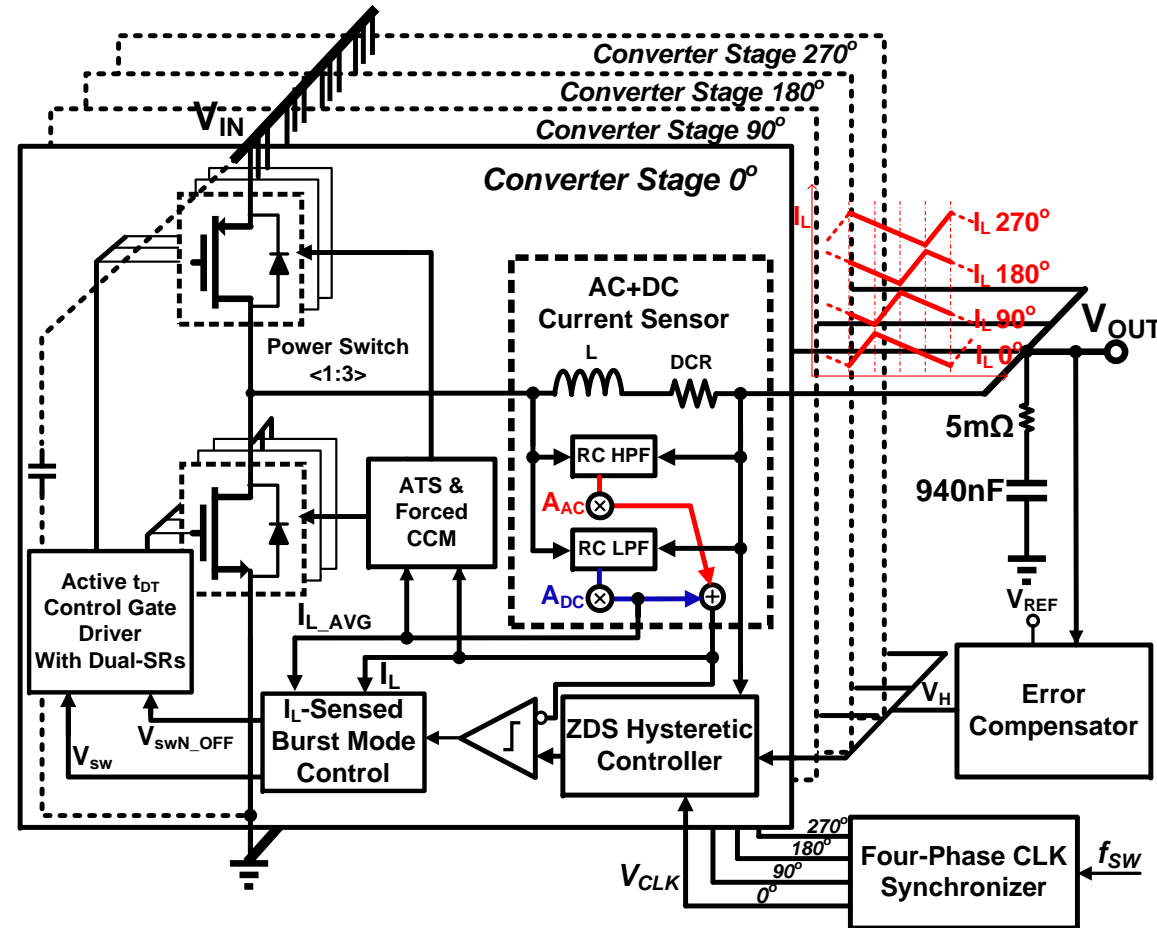


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- Before ATS stages 2,3 (V_{GPH}, V_{GNH}) are completely shut off due to the I_o step-down, they momentarily remain in CCM until I_{L_AVG} hits I_{ATS} .
- During this forced-CCM time, the converter temporarily allows a negative I_L , quickly discharging residual charge left on C_o .

Outline

- Background and Challenges
- Proposed Design
 - Control Scheme : Zero Delay Response
 - Control Scheme : f_{sw} Synchronization
 - Emulated AC+DC Current Sensing
 - Wide Range Efficiency
- **Four-Phase System Architecture**
- Measurement Results
- Comparison and Conclusion

Four-Phase System Architecture

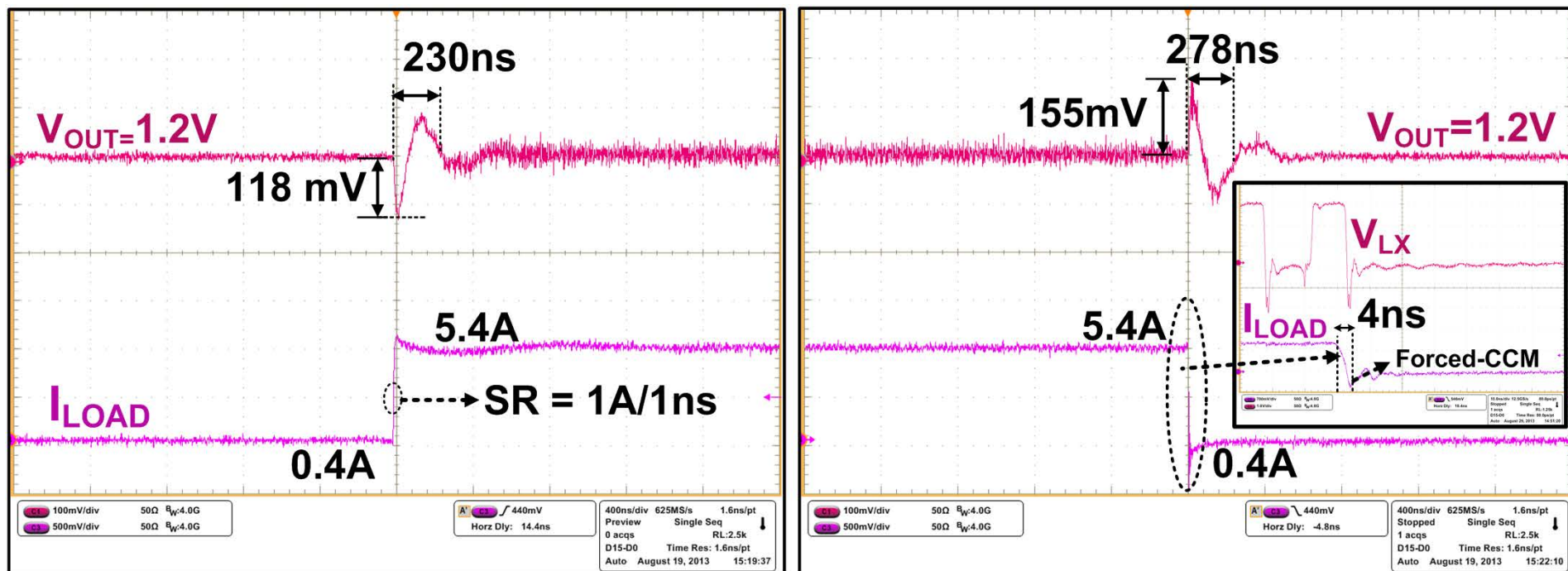


- ZDS Hysteretic Control
- 4-phase synchronization
- Cycle-by-cycle current sharing.
- Ultra-low ESR of $5m\Omega$.
- C_O of only $940nF$ for $5A/5ns$ I_O transient.
- I_L -sensed burst mode control
- Adaptive transistor sizing with forced-CCM

Outline

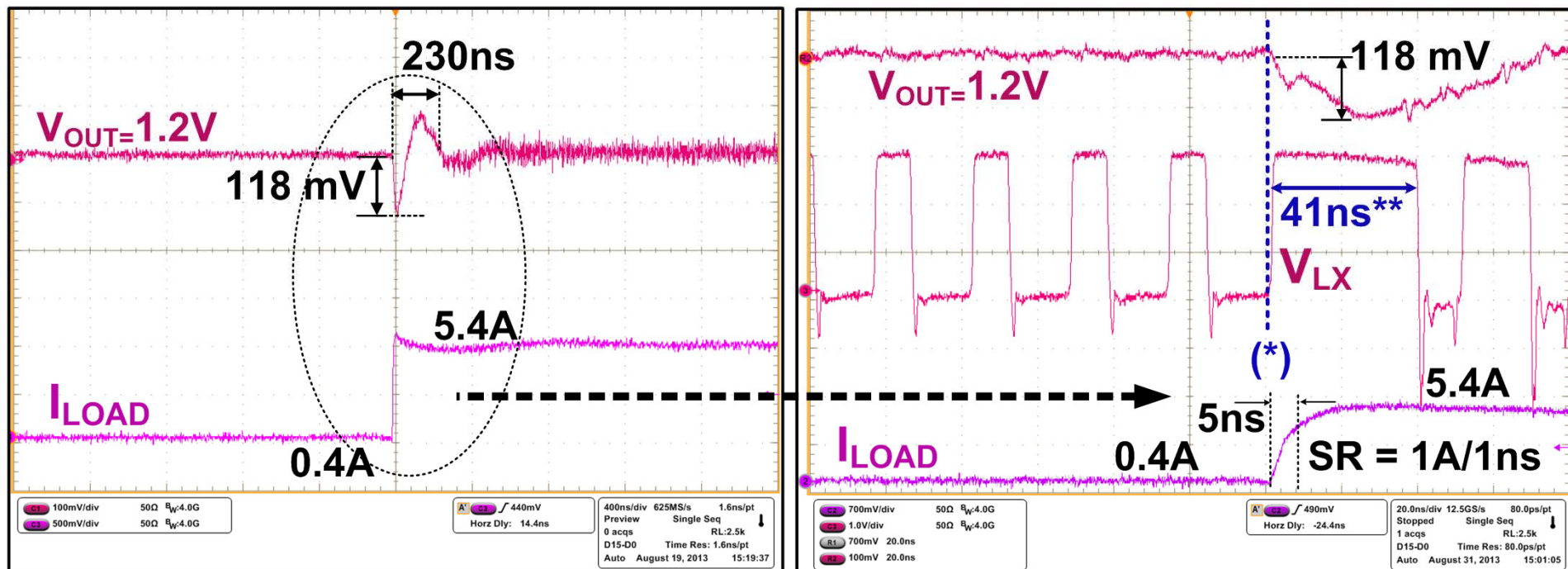
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Results: Transient Response



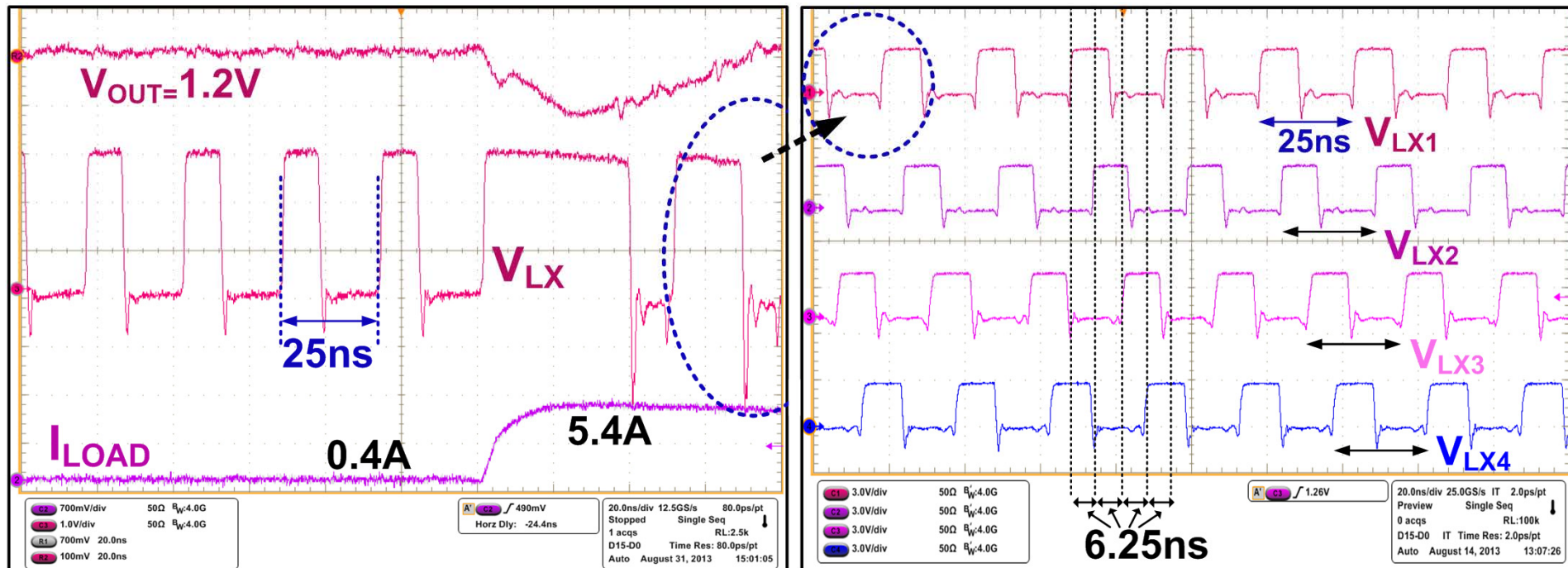
- 5A load step with $>1\text{A}/1\text{ns}$ slew rate is tested with $2 \times 470\text{nF}$ ($10\text{m}\Omega$ ESR) filtering output capacitor.
- Forced-CCM operation is temporarily active during the I_o step down.

Results : ZDS Hysteretic Behavior



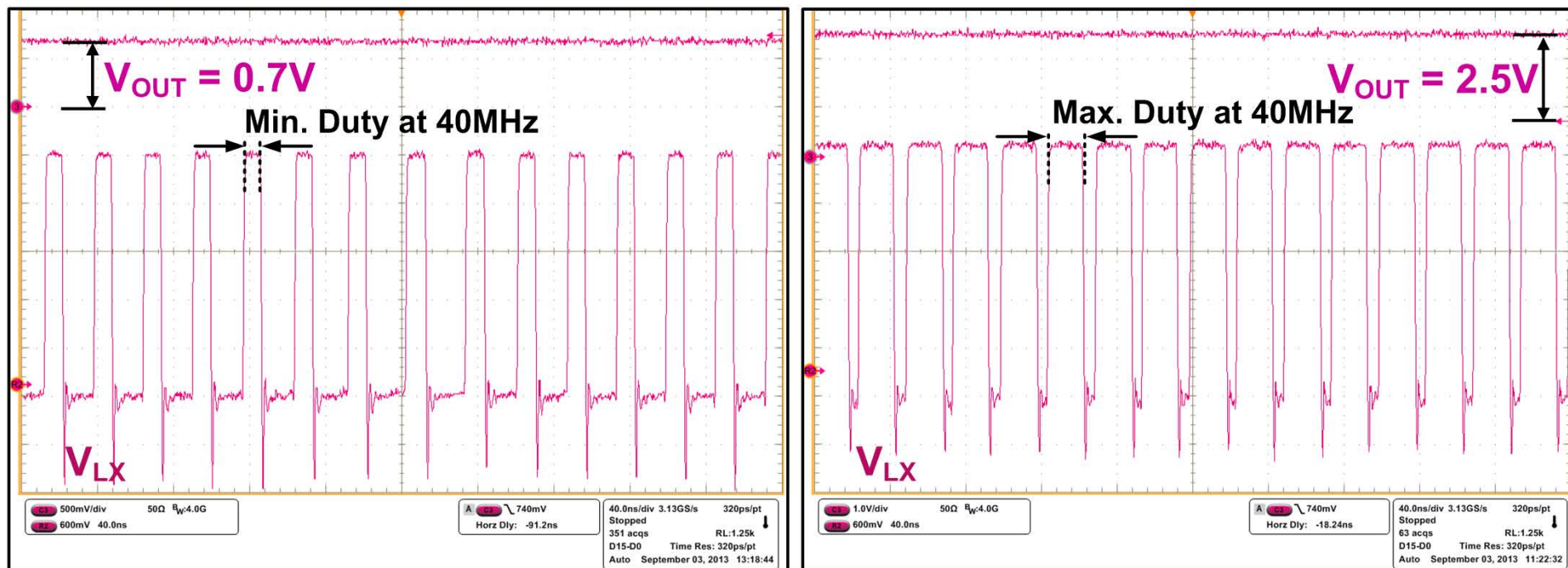
- ZDS hysteretic control turns V_G on instantly* in response to a I_O step up.
- Duty ratio is saturated with V_G on-time of 41ns**, which is the equivalent time for I_O to rise by 4.8A.

Results : Four-Phase Synchronization



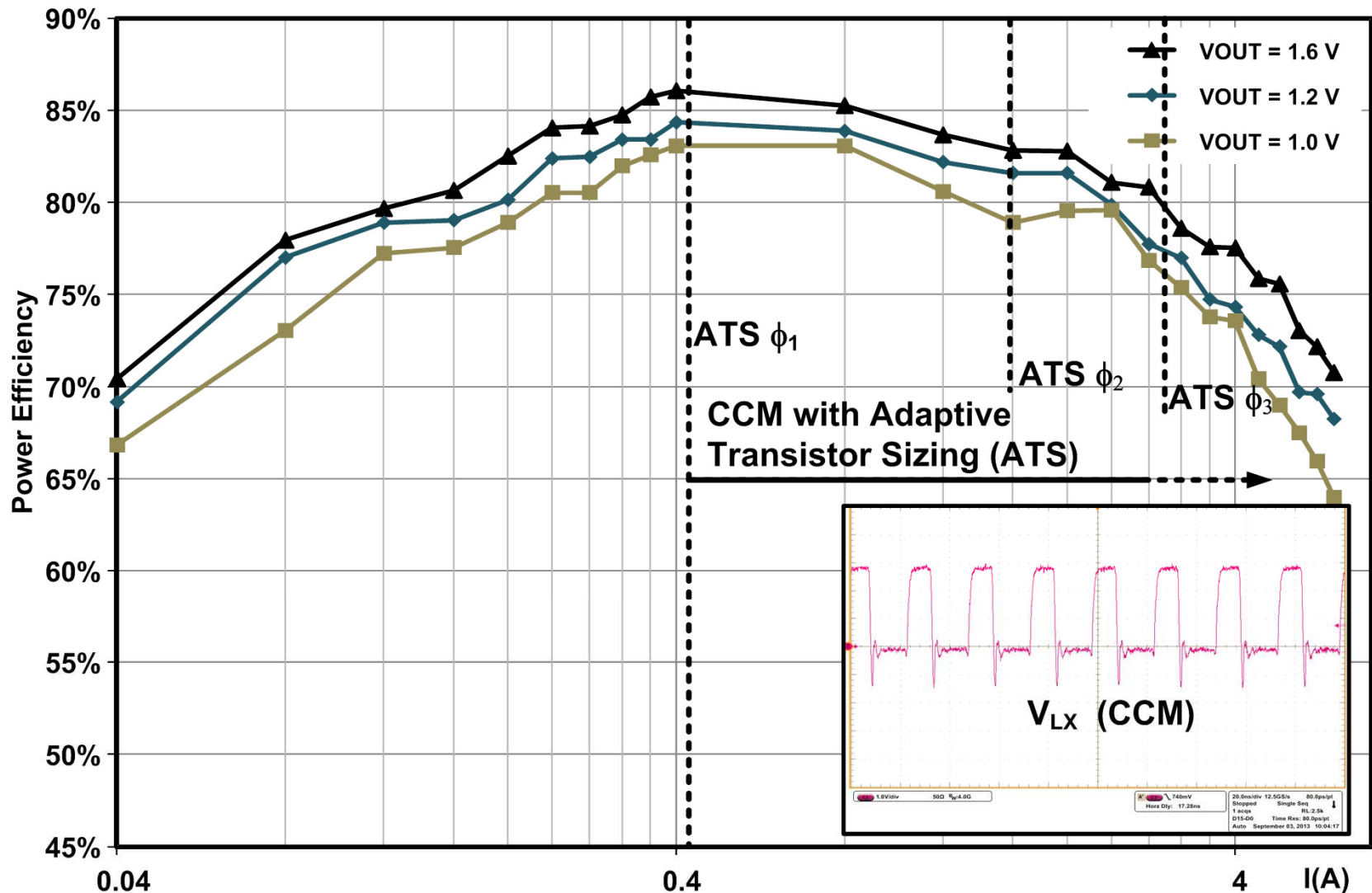
- At the moment of the I_O step-up, switching synchronization to the programmed clock is lost due to ideal hysteretic behavior.
- After the I_O step-up, the switching is re-synchronized to 40MHz, with 4-phase synchronization.

Results : Hysteretic Based ZDS Control

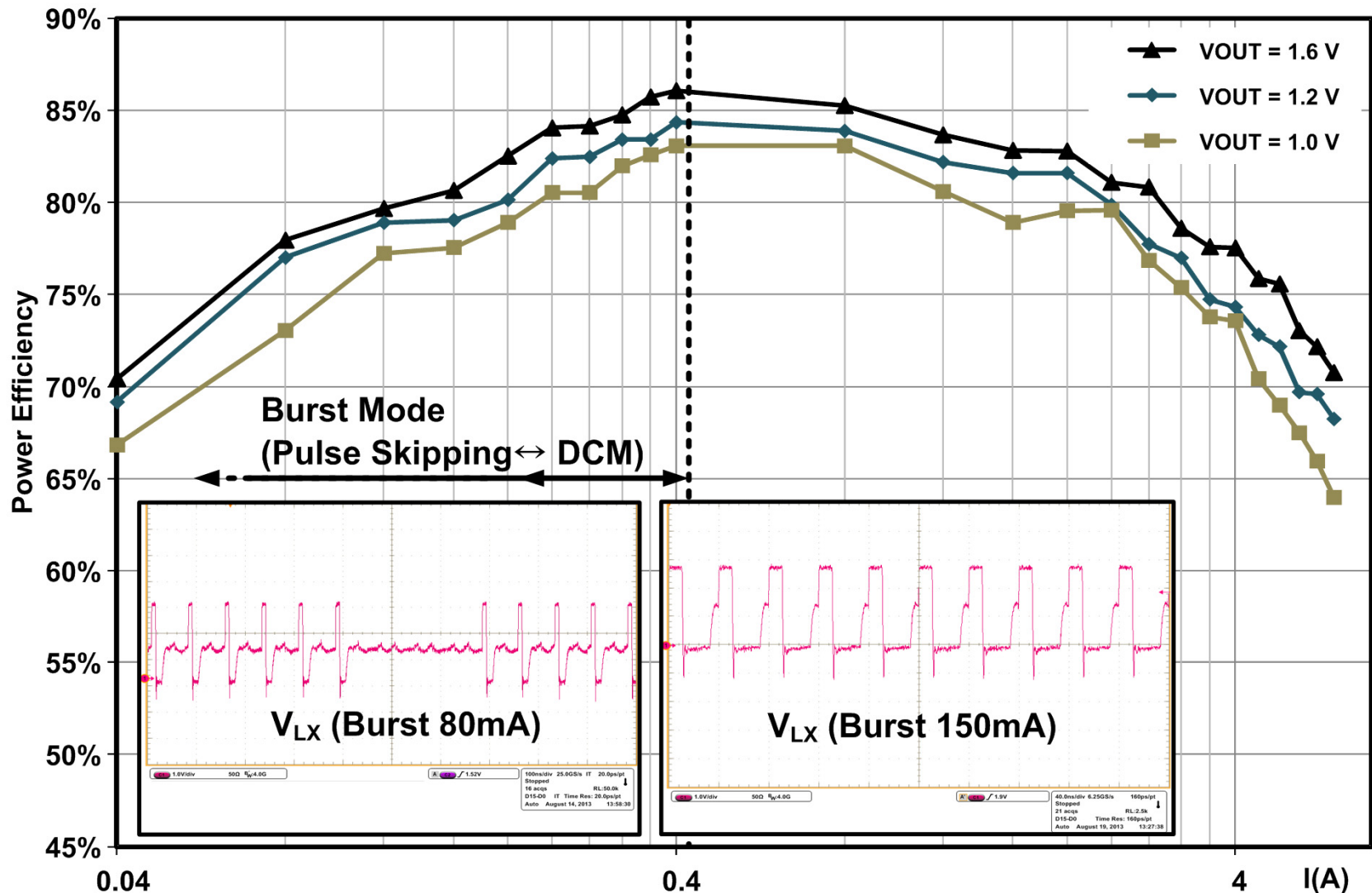


- Hysteretic-based control exhibits no duty ratio limitations like PWM current mode control.
- At 40MHz, the duty ratio can adjust V_O from 0.7~2.5V from 3.3V V_{IN} .

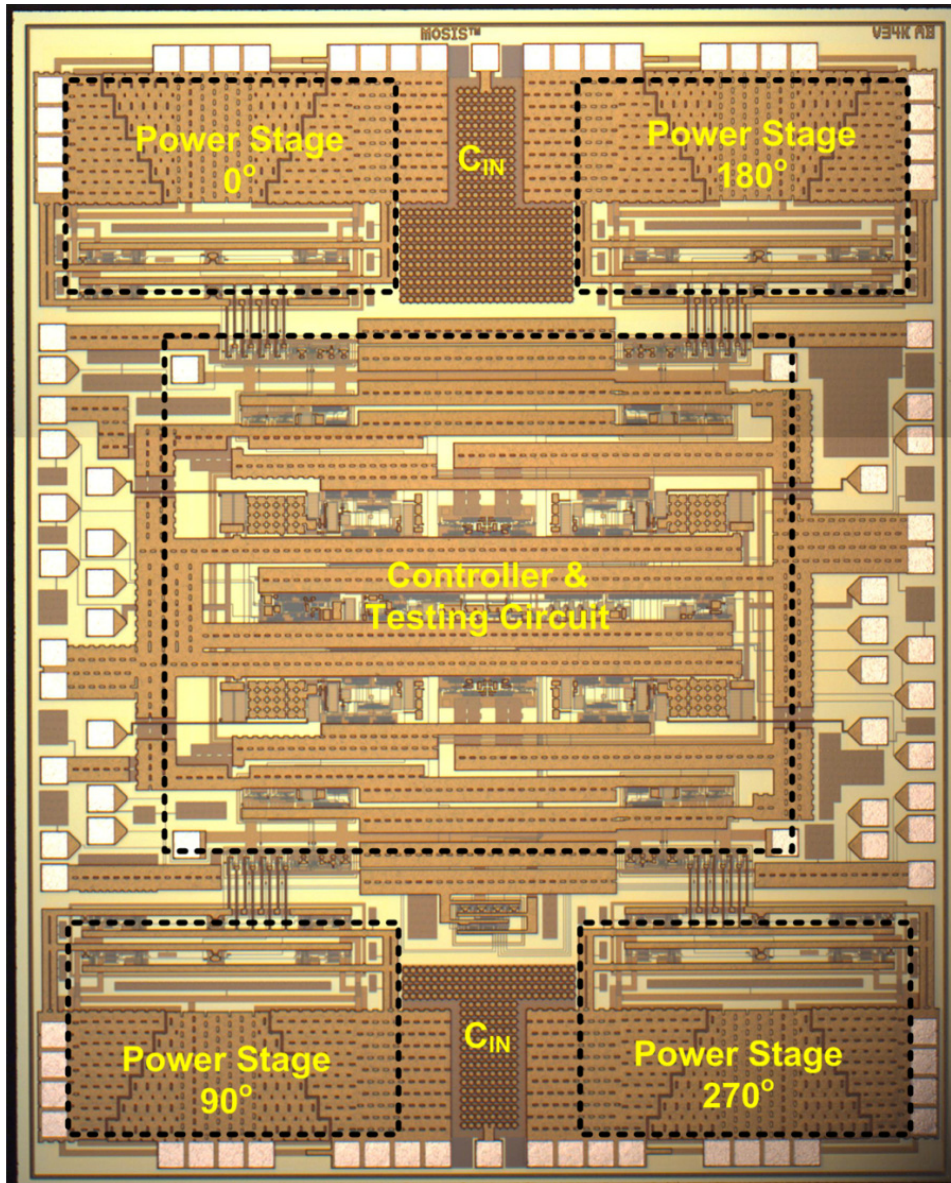
Efficiency with ATS



Efficiency with Burst Mode Control



Chip Micrograph



- TSMC 0.18 μ m CMOS process
- Chip area: 2.5mm \times 3.1mm (including test circuits)
- 2nF of on-chip V_{IN} decoupling capacitor

Outline

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Performance Comparison

	ISSCC '13 [1]	JSSC '05 [2]	JSSC '09 [3]	This Work
Control	PWM	Hysteretic	Hysteretic	ZDS Hysteretic
Current Sharing	Master-Slave	Cycle-by-Cycle	None	Cycle-by-Cycle
$V_{IN (MAX)}$ (V)	1.2	1.2	4.9	3.3
V_{OUT} (V)	0.6-1.05	0.9	0.86-3.93	0.7-2.5
f_{SW} (MHz) (phases)	100 ($\times 4$)	233 ($\times 4$)	32-35 ($\times 4$)	40 ($\times 4$)
L (nH)	8	6.8	110	78
C_{OUT} (μF)	0.00187	0.0025	0.2	0.94
I_{MAX} (A)	1.2	0.3	1	6
Load Step (mA/ns)	180 / 800	150 / 0.1	300 / 30	5000 / 5
1% t_{settle} (ns)	~2000	~30	~350	230
V_{OUT} Droop (%)	6.7% ($V_{OUT}=0.9V$)	10% ($V_{OUT}=0.9V$)	10% ($V_{OUT}=1.8V$)	9.8% ($V_{OUT}=1.2V$)
Peak Efficiency (%)	82.4	83.2	80	86.1

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- ZDS hysteretic control enables:
 - Ideal near zero-delay response to I_o transients
 - 4-phase synchronization with cycle-by-cycle current sharing.
 - **6× lower f_{sw}** for comparable response to prior art.
 - Lower f_{sw} facilitates higher efficiency at **2× lower conversion ratio** and enables larger **I_{MAX} of 6A.**

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- Emulated AC+DC current sensor enables the use of 78nH inductors with ultra-low 42mΩ DCR.
- **86.1% peak efficiency is achieved.**
- **Wide range efficiency is enabled by burst-mode control and ATS.**

Acknowledgements

This work is jointly supported by the U.S. National Science Foundation under the research contracts CCF-0844557 and DGE-1147385.

For their invaluable support and feedback, a special thanks to

Texas Instruments

- Brian Crutcher
- Jeff Morroni
- Mark Morgan
- Pooya Forghani

AMD

- Steve Kosonocky

Freescale

- John Pigott

Intel

- Harish Krishnamurthy

An 87%-Peak-Efficiency DVS-Capable Single-Inductor 4-Output DC-DC Buck Converter with Ripple-Based Adaptive Off-Time Control

Danzhu Lu, Yao Qian, Zhiliang Hong

State Key Laboratory of ASIC and System, Fudan University, Shanghai, China



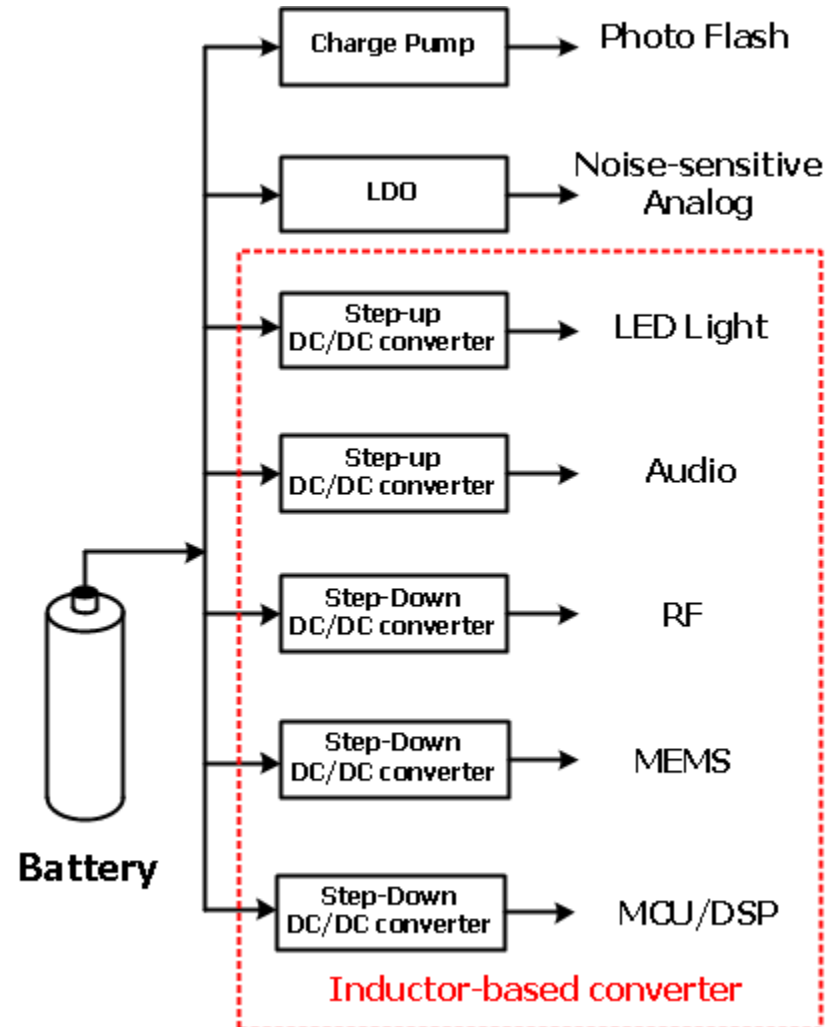
Department of Microelectronics, Fudan University

Outline

- **Motivation**
- **Previous research of SIMO converters**
- **System design of ripple-based Adaptive Off-time control method**
- **Schematics Design**
- **Measurement Results**
- **Q & A**

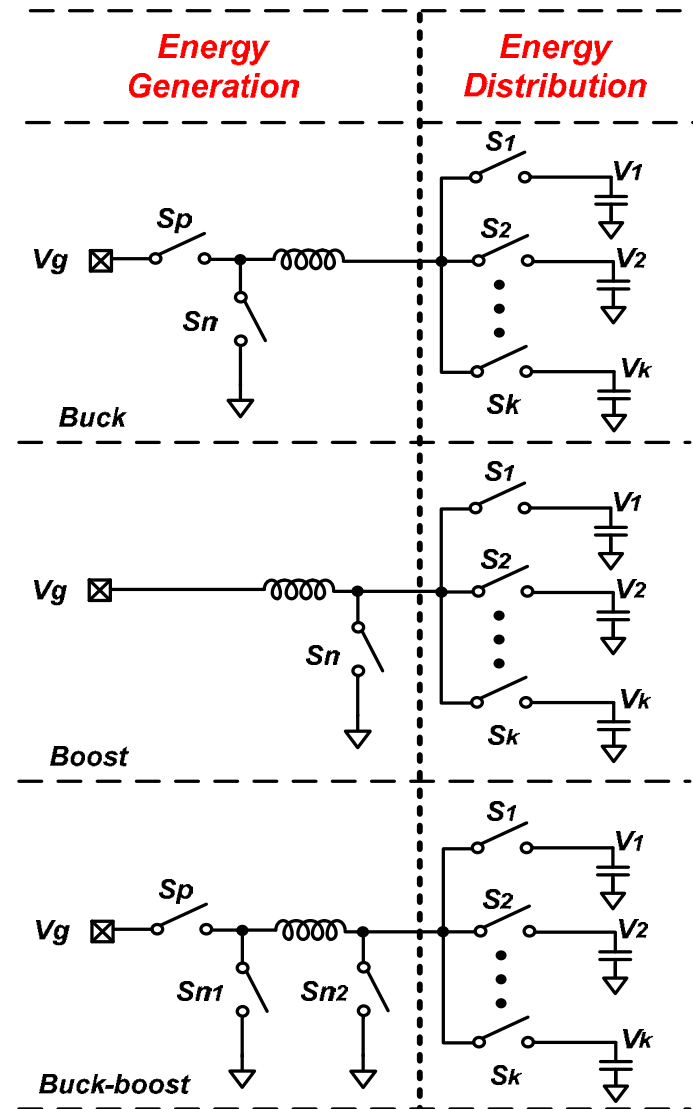
Motivation

- Multiple Inductor-based DC-DC converters are required in portable devices power management
- SIMO converter can support several outputs with one inductor to save the PCB area and production cost



Motivation

- Power stage structure of SIMO converter
- Advantages
 - Area-saving
 - High power density
- Disadvantages
 - Large ripple
 - Cross regulation
 - Low efficiency

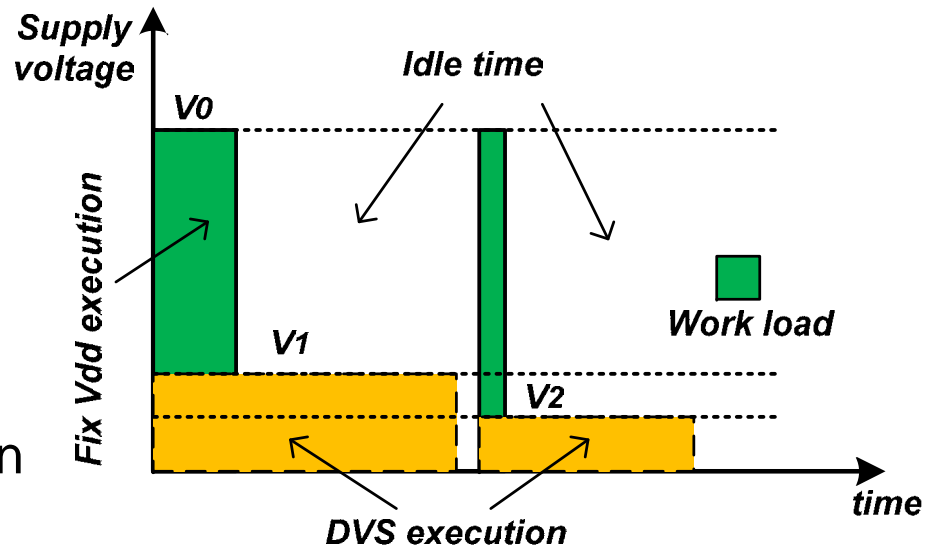


Motivation

- **Dynamic voltage scaling (DVS) technique**

- **Advantages**

- Supply voltage of micro-processors can be adjusted depending on the specific needs during execution to save the power consumption

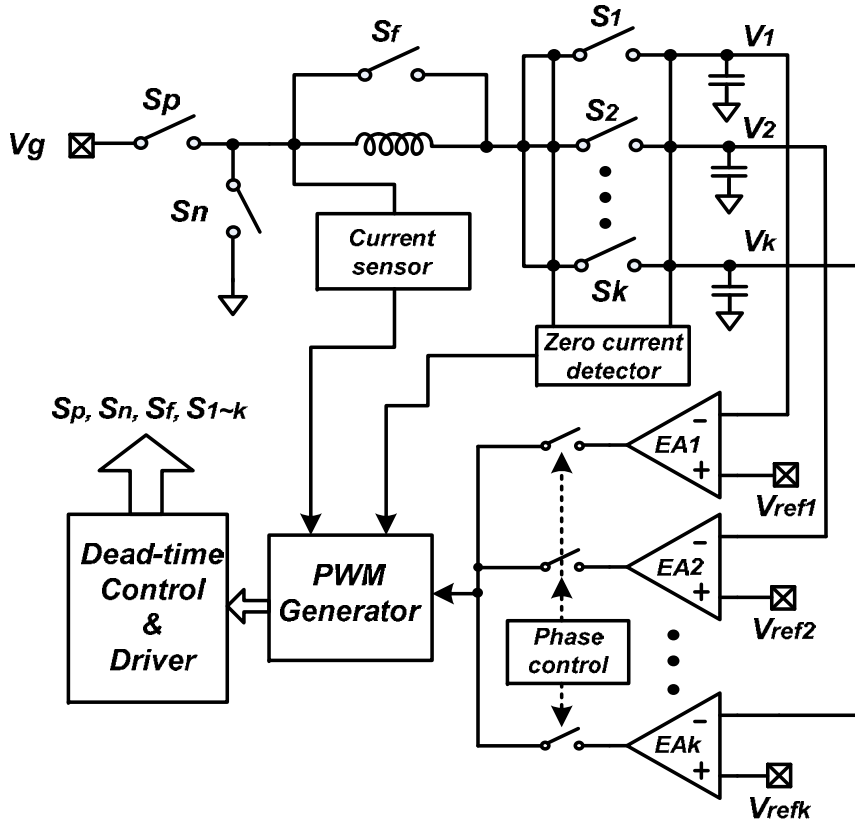


- **Cross-regulation and slow response speed also limit its application in SIMO converters**

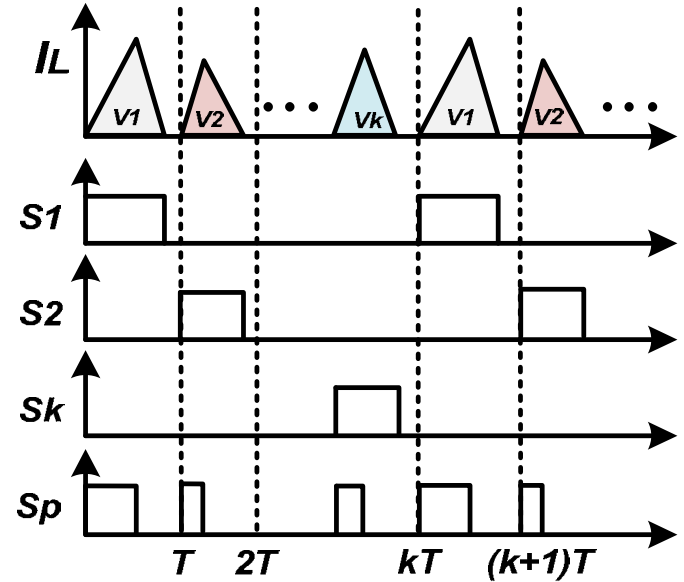
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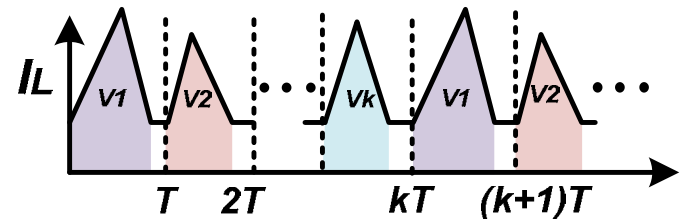
Time-multiplexing control



- **No cross regulation**
- **Large ripple**
- **Low response speed**
- **Low current capability**

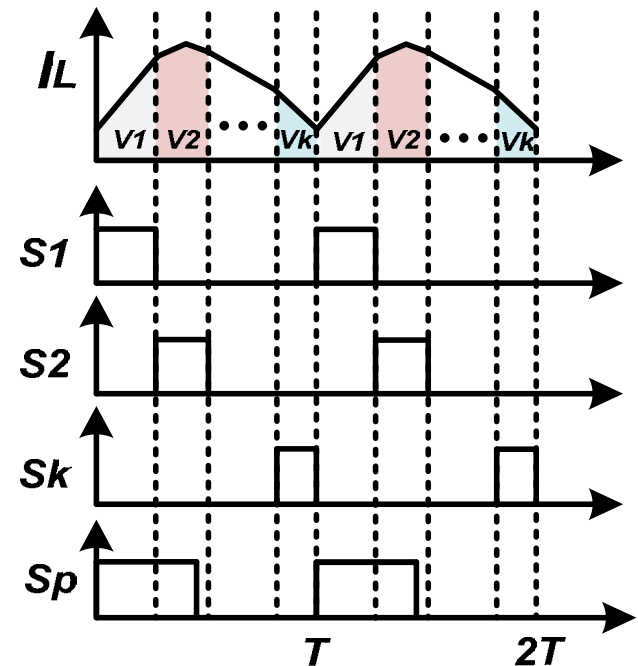
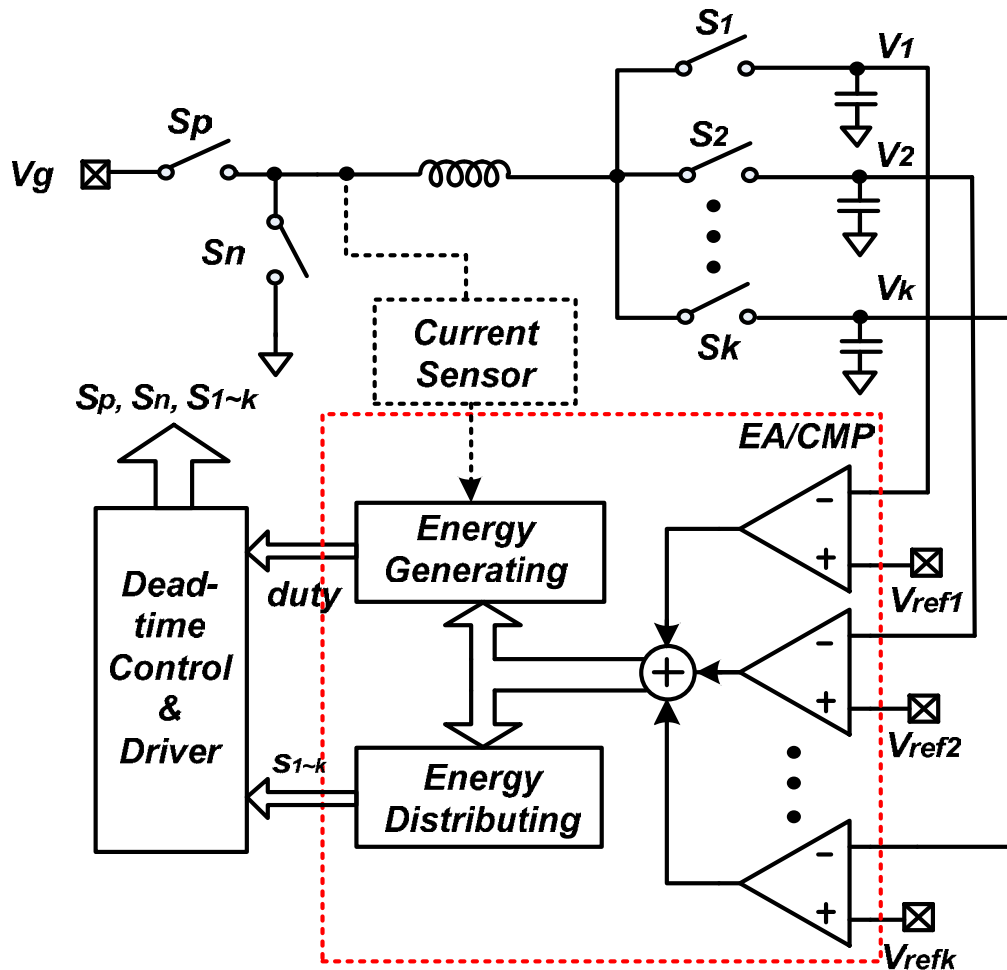


Pseudo-CCM with Freewheel Switching



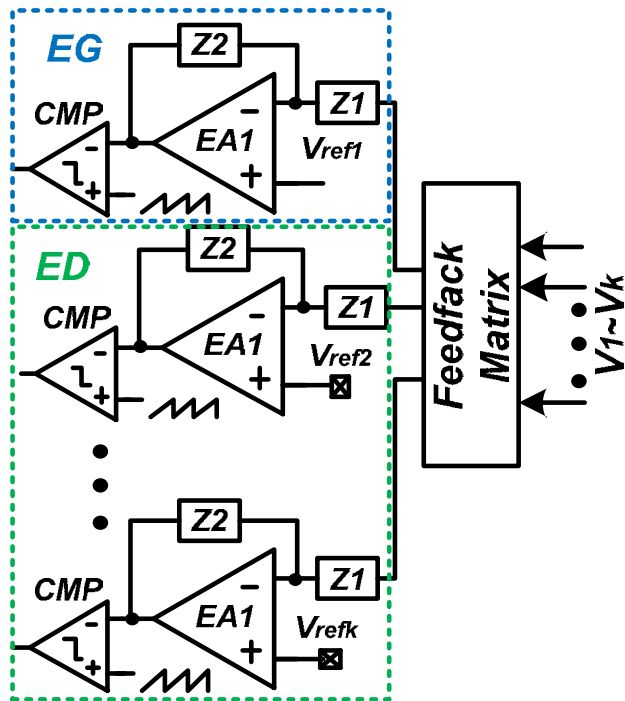
ISSCC 2002 [1]

Single-charging control

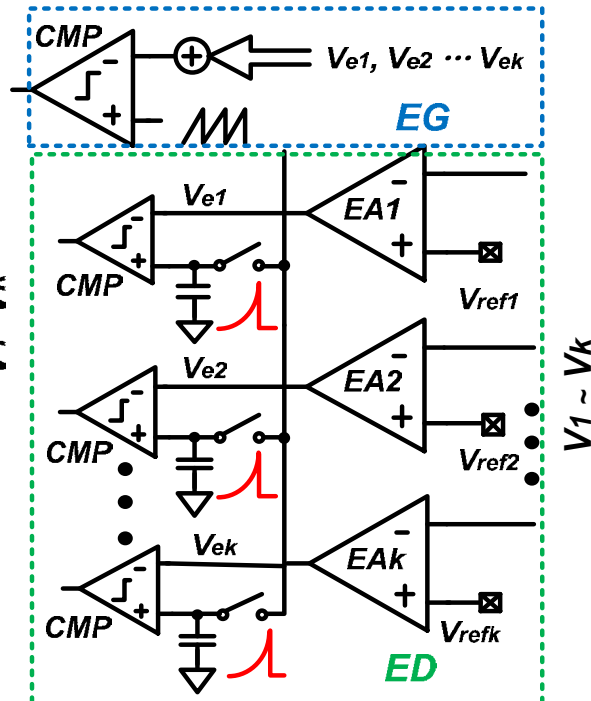


- Small ripple
- Large current
- Cross regulation

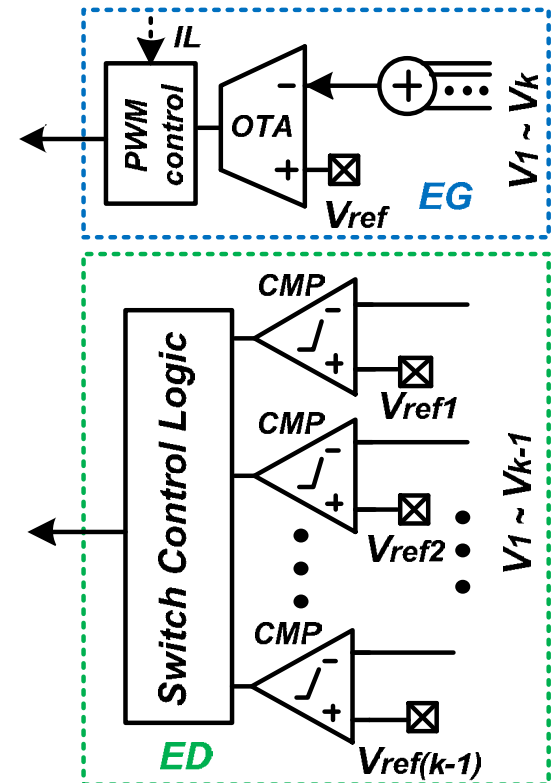
Single-charging control



PWM control
ISSCC 2008 [2]



Charge Control
ISSCC 2012 [3]



Comparator-based Control
ISSCC 2010 [4]

- **Small ripple**
- **Poor cross regulation**
- **Low response speed**

- **Little cross regulation**
- **Low efficiency**
- **Low response speed**

- **Easy to realize**
- **Fast response speed**
- **Poor cross regulation**

Summary

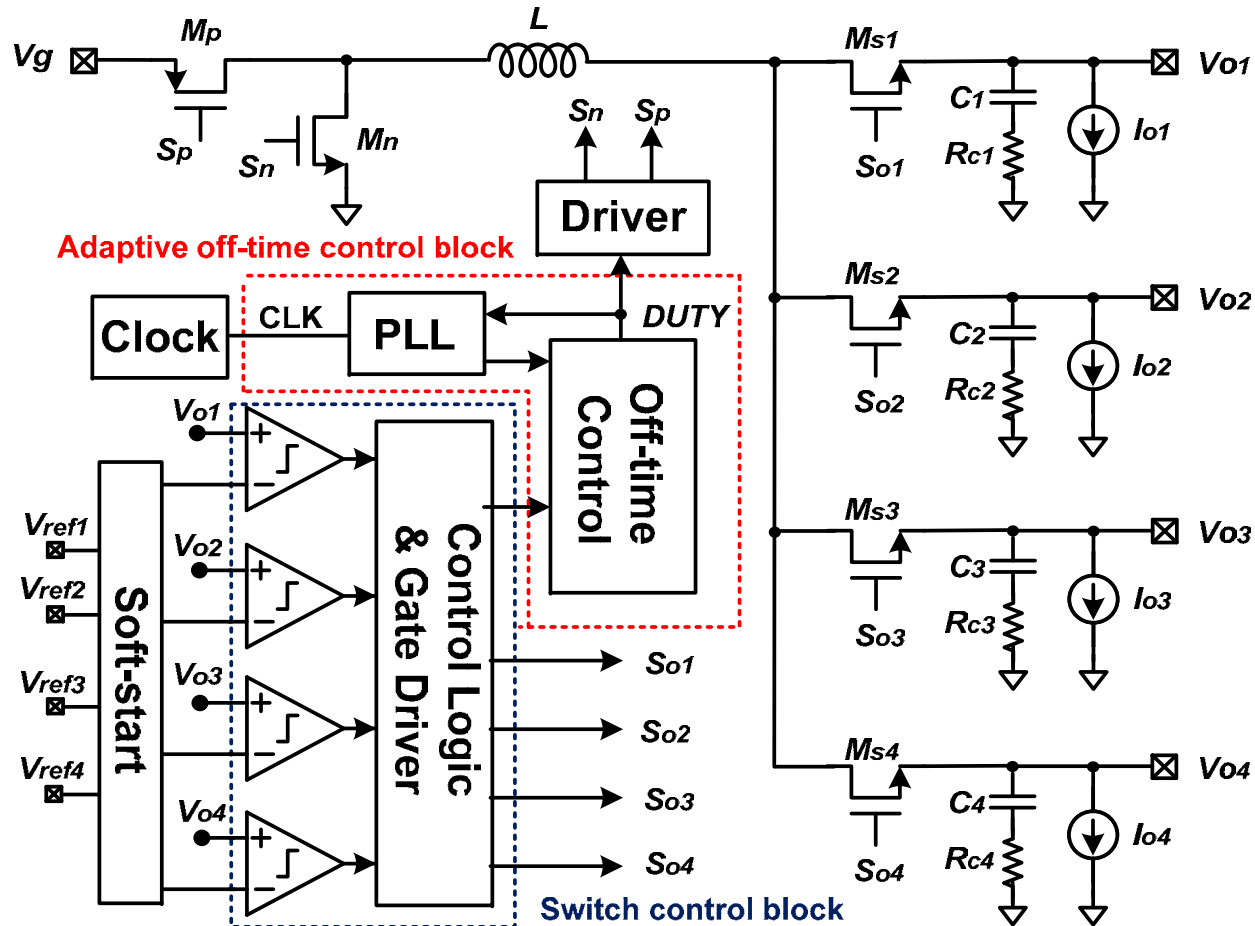
Control method	Time-multiplexing	Single-charging		
		Comparator-based	PWM loop	Charge control
Output ripple	High	Low	Low	Low
Current capability	Low	High	High	High
Response speed	Low	Medium	Low	Low
Cross Regulation	Low	High	High	Low
Efficiency	Low	High	High	Low
Complexity	Low	Medium	Medium	High

- **High efficiency and low cross regulation cannot be achieved simultaneously**
- **High Response speed cannot be realized in all channels**

Outline

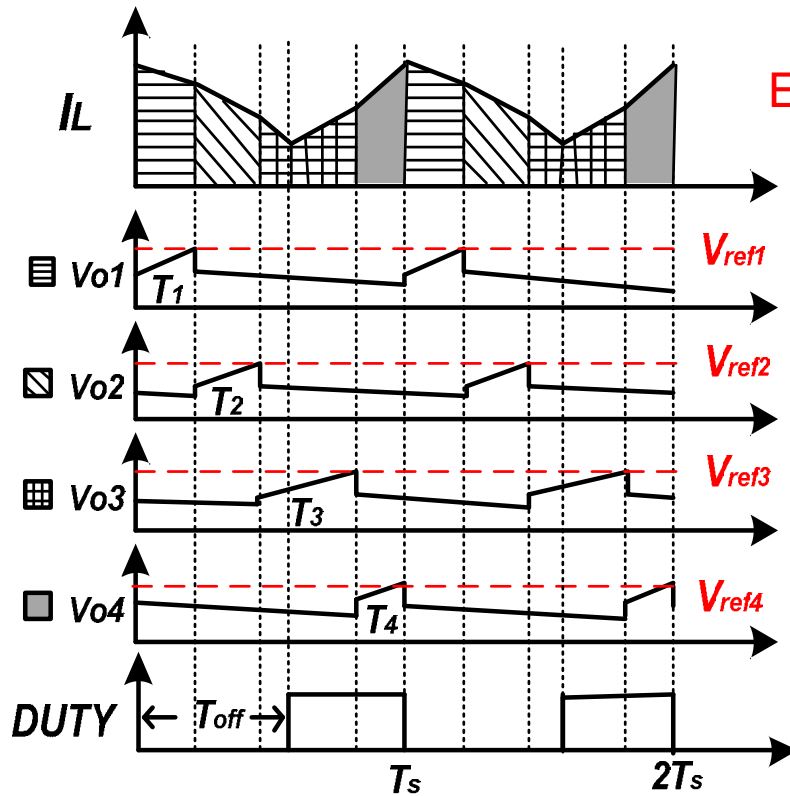
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RBAOT control



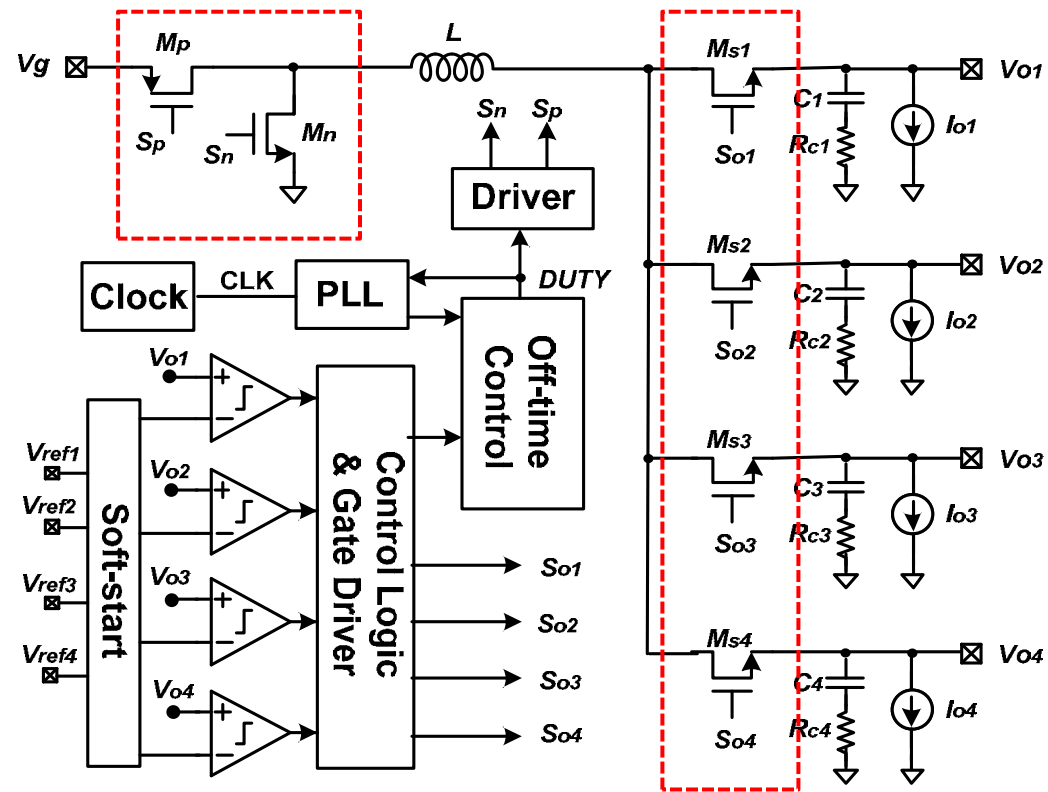
- No compensation required, so response is fast
- Achieve high efficiency and low cross regulation

Steady-state response



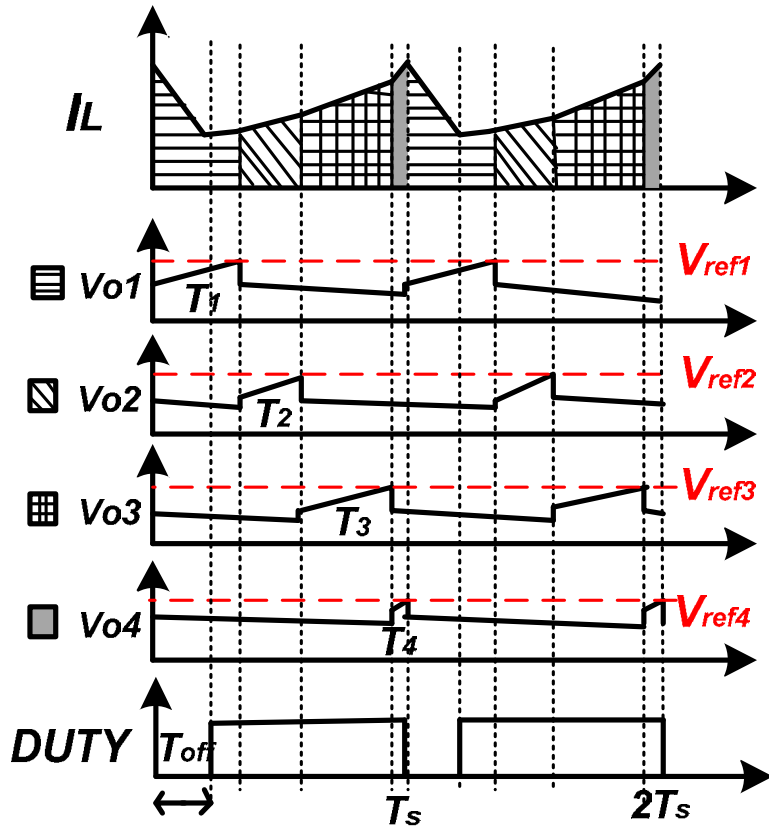
$$\bar{V}_{out} = \frac{\frac{V_{o1}^2}{R_1} + \frac{V_{o2}^2}{R_2} + \frac{V_{o3}^2}{R_3} + \frac{V_{o4}^2}{R_4}}{\frac{V_{o1}}{R_1} + \frac{V_{o2}}{R_2} + \frac{V_{o3}}{R_3} + \frac{V_{o4}}{R_4}} \quad D = \frac{\bar{V}_{out}}{V_g}$$

Energy generation switch

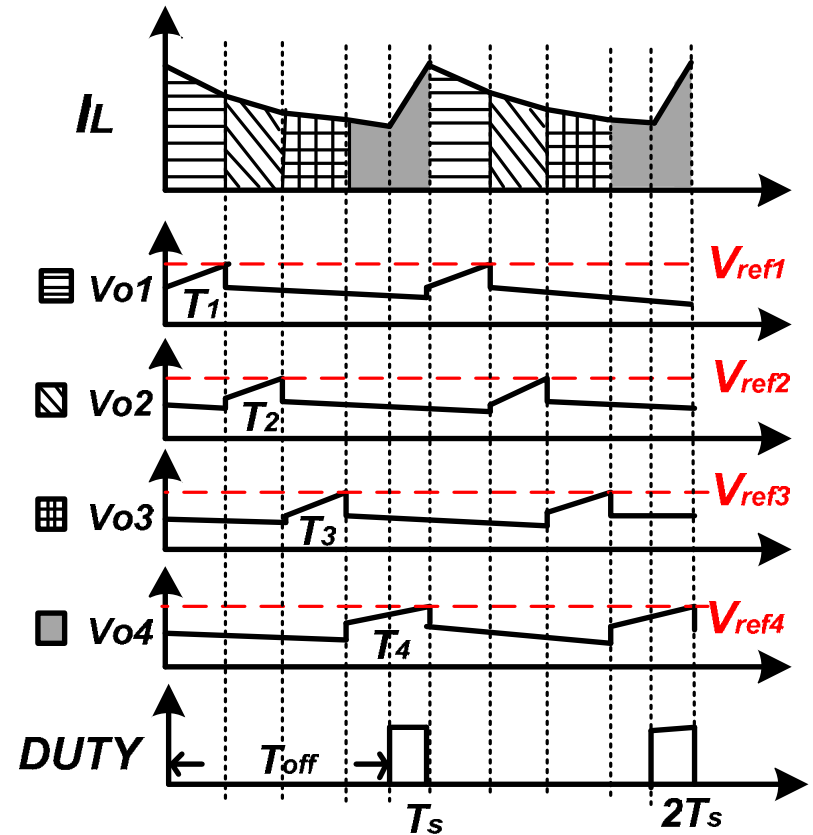


Energy distribution switch

Steady-state response



With large duty cycle

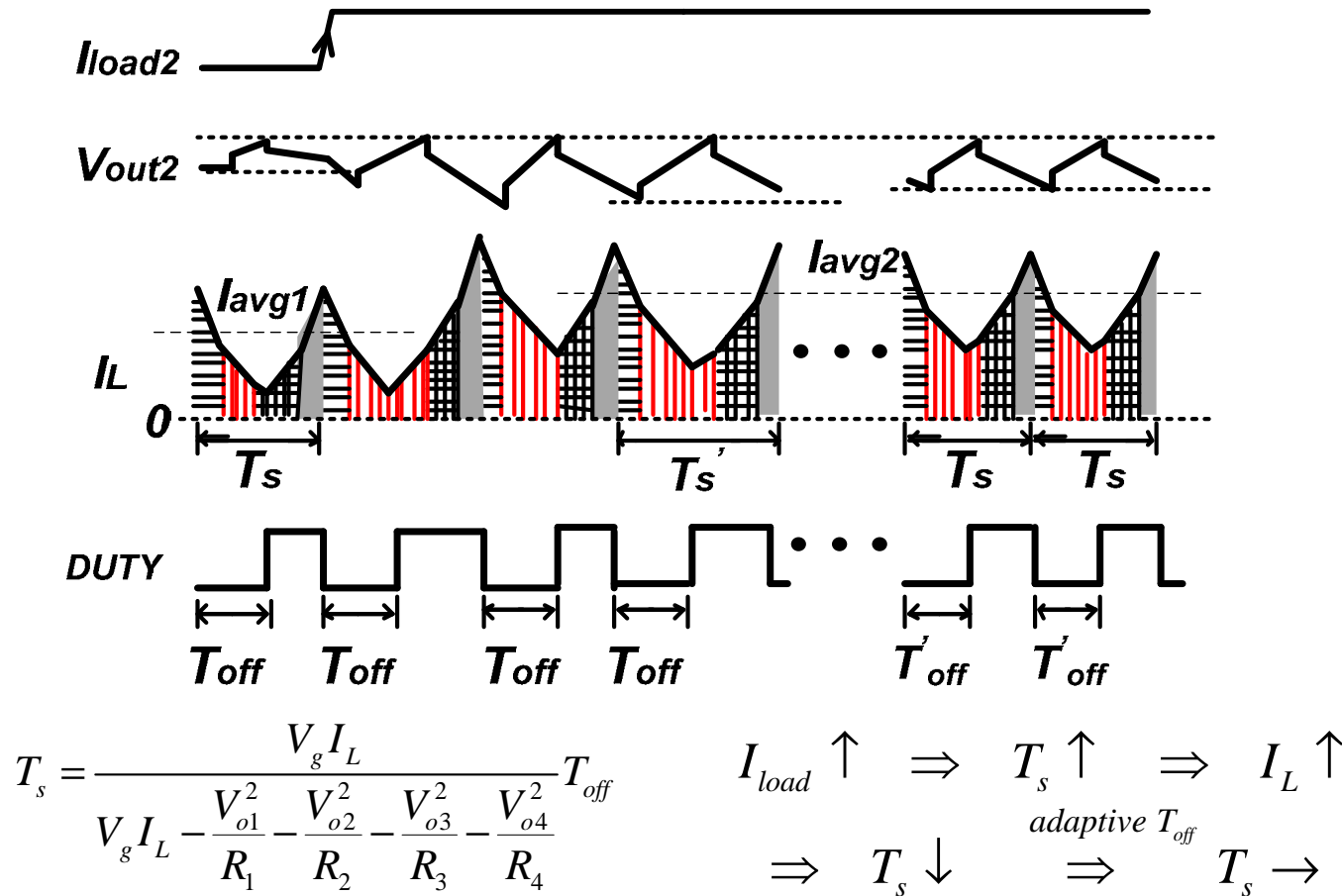


With small duty cycle

$$V_{oi} = \frac{T_i R_i (T_s - T_{off})}{T_1^2 R_1 + T_2^2 R_2 + T_3^2 R_3 + T_4^2 R_4} V_g \quad (i=1 \sim 4)$$

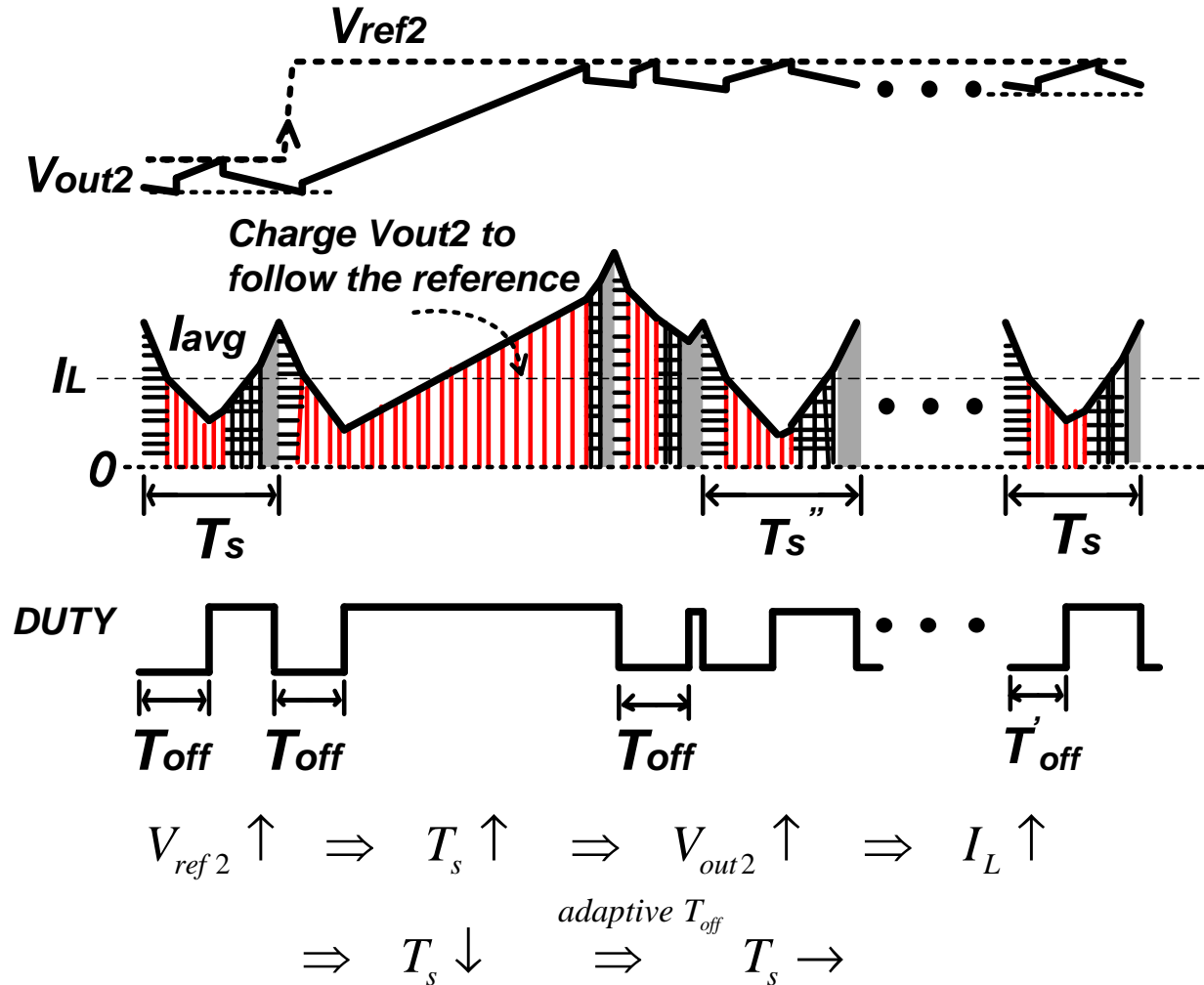
$$I_L = \frac{V_{o1}}{R_1} + \frac{V_{o2}}{R_2} + \frac{V_{o3}}{R_3} + \frac{V_{o4}}{R_4}$$

Load Transient Response



- Modify the I_L with period adjustment
- Fast response speed and low cross-regulation

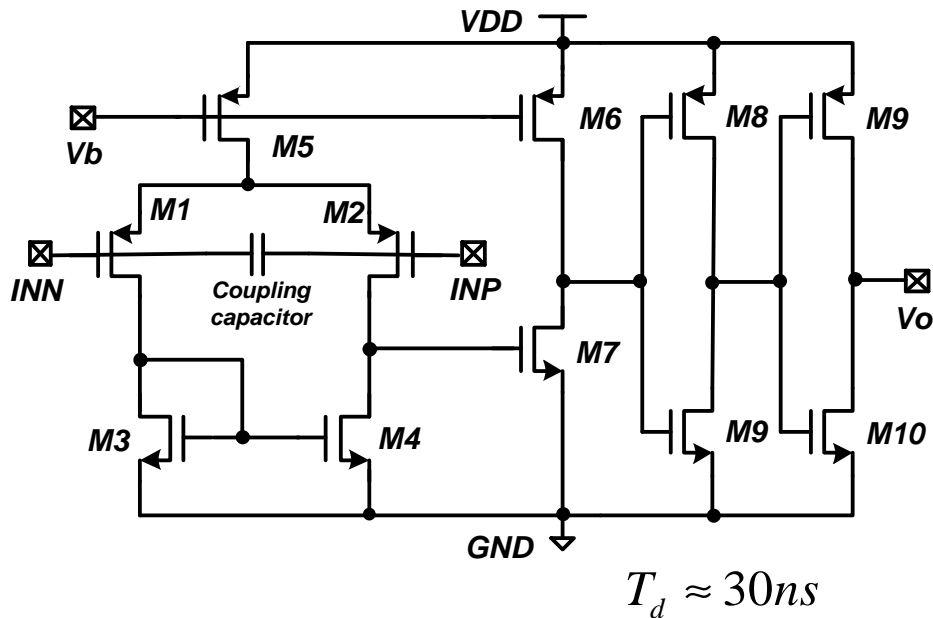
DVS Transient Response



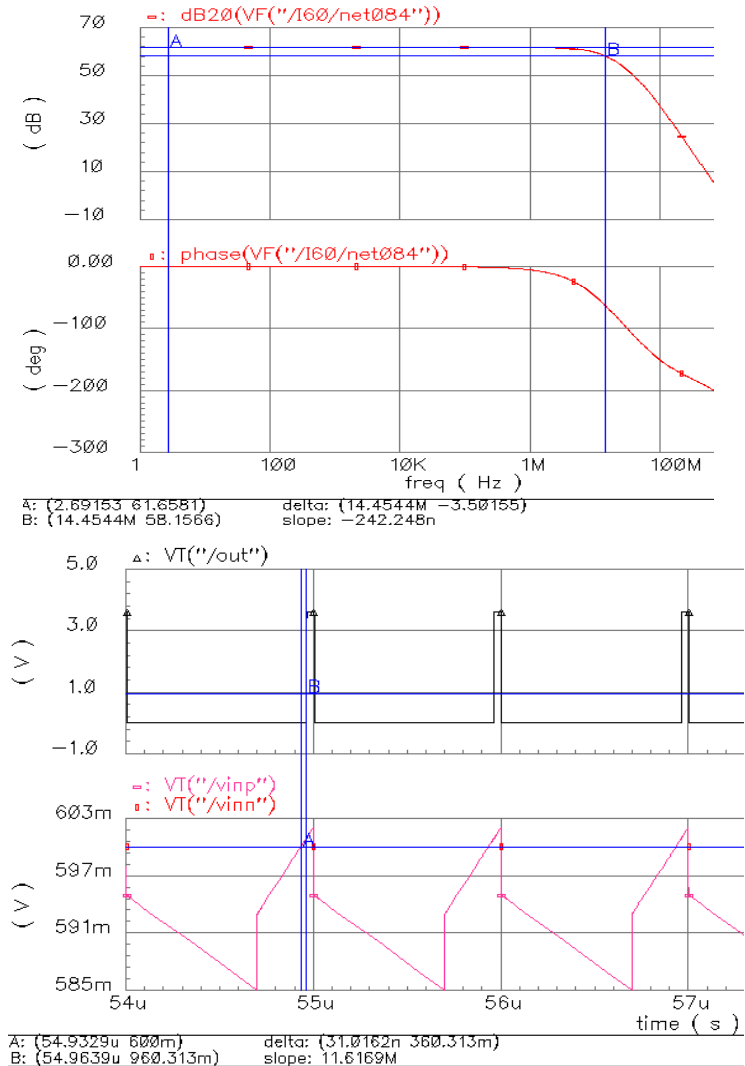
Outline

- Motivation
- Previous research of SIMO converters
- System design of ripple-based Adaptive Off-time control method
- **Schematics Design**
- Measurement Results
- Q & A

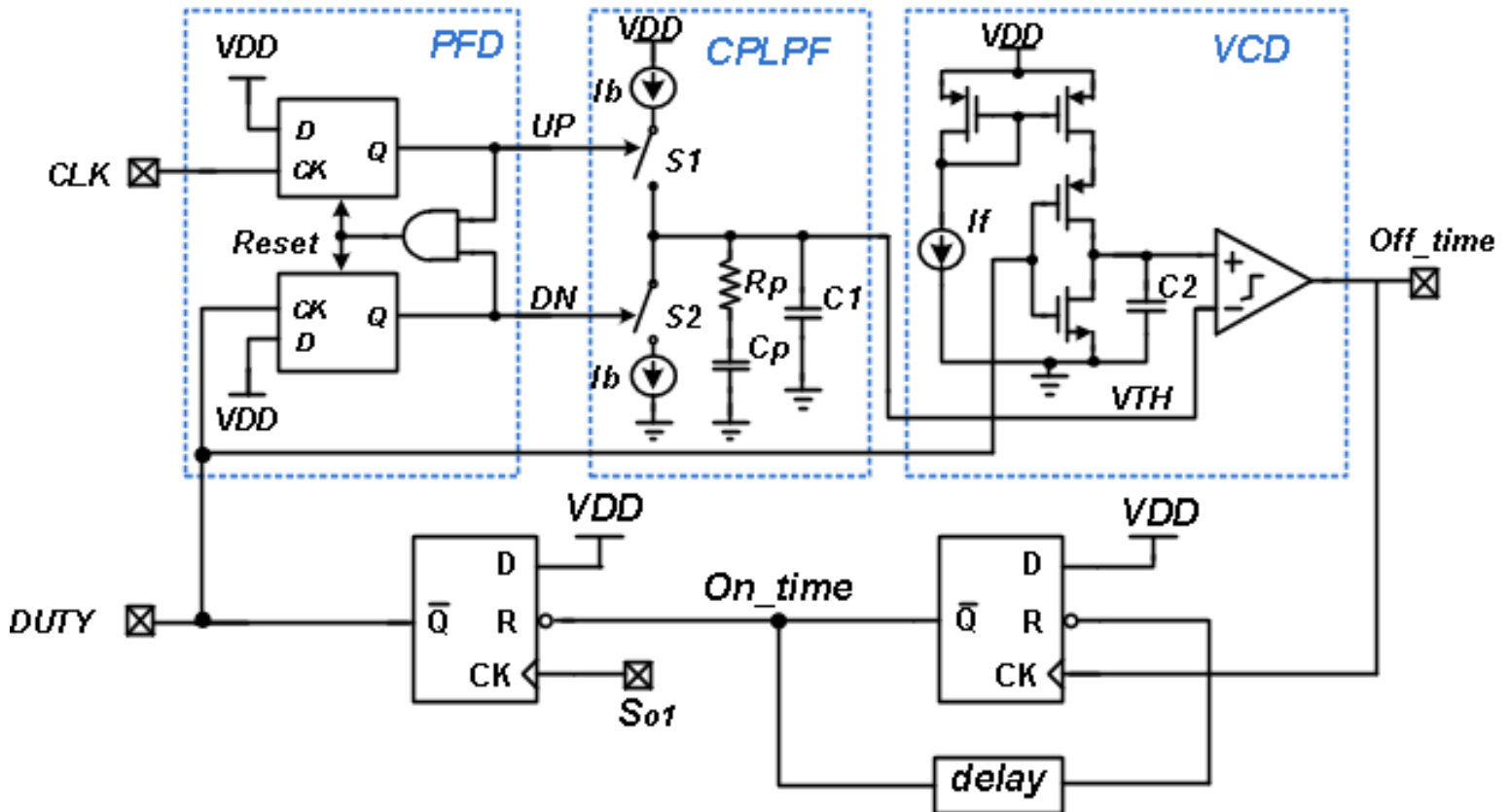
Comparator



- Coupling capacitor is used to remove the influence of spikes
- The rising and falling edge delays are not equal



PLL control loop

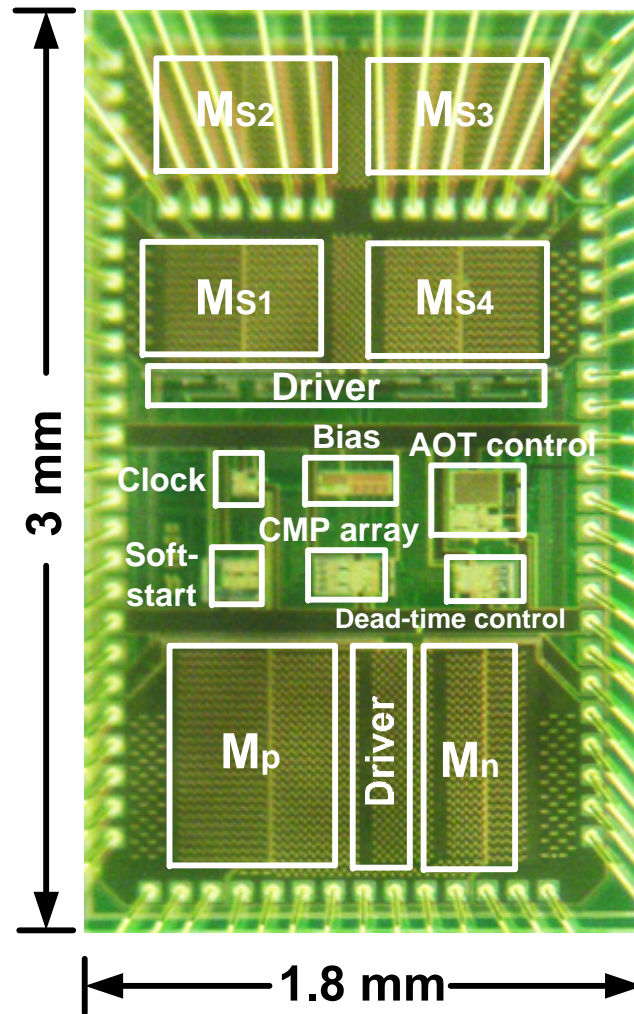


$$G(s) = \frac{I_b C_2 (V_g - \bar{V}_{out})}{I_f \bar{V}_{out} T_s^2} \frac{1 + s C_p R_p}{s^2 (s R_p C_p C_1 + (C_p + C_1))} \quad GBW \approx 100kHz$$

Outline

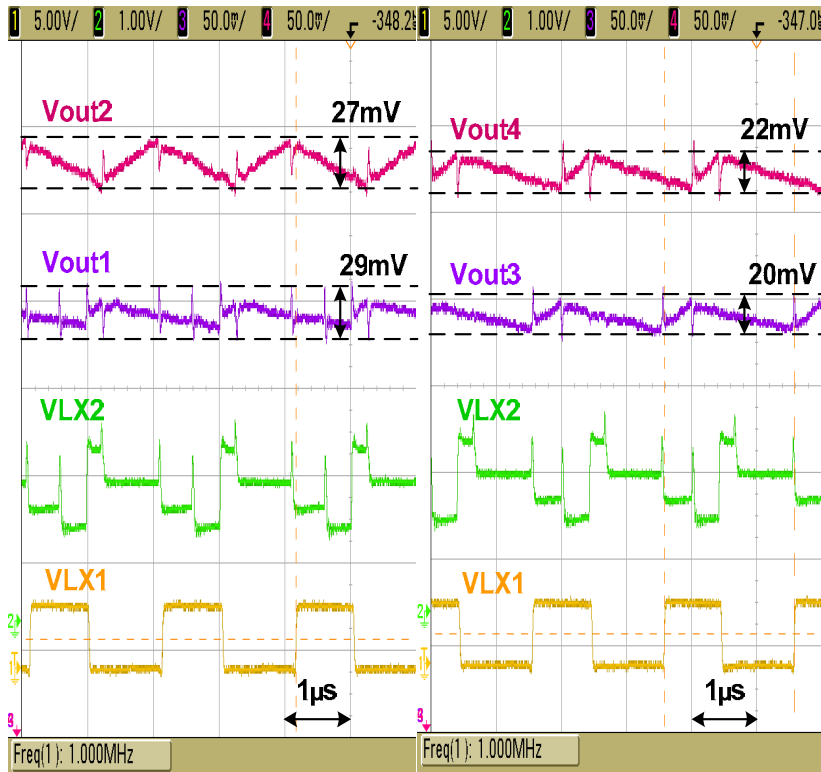
- Motivation
- Previous research of SIMO converters
- System design of ripple-based Adaptive Off-time control method
- Schematics Design
- **Measurement results**
- Q & A

Chip

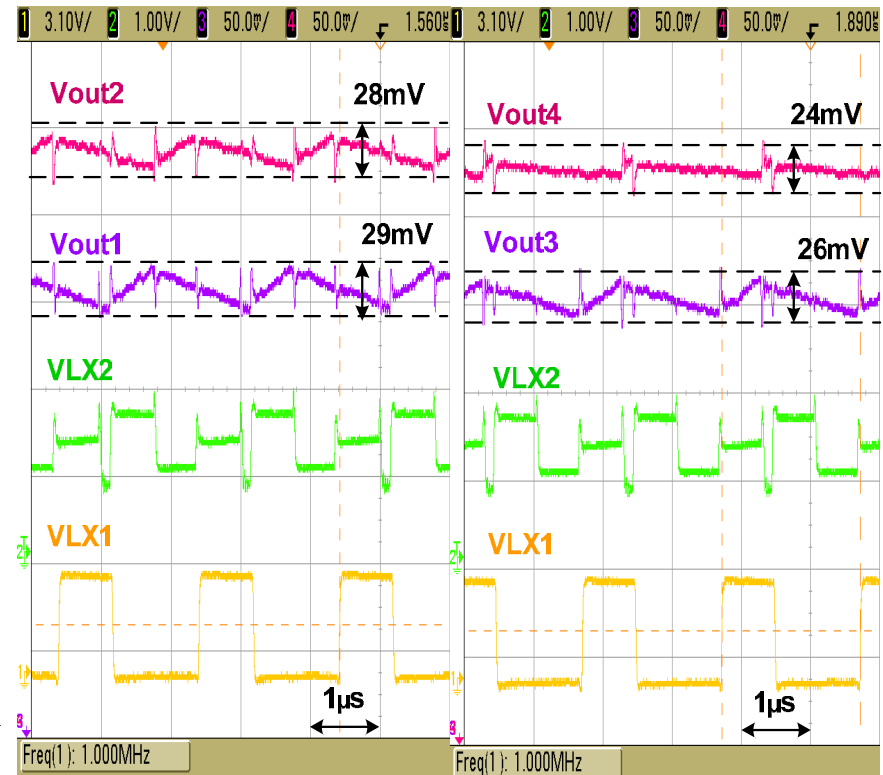


GF 0.35 μ m CMOS

Steady-state response

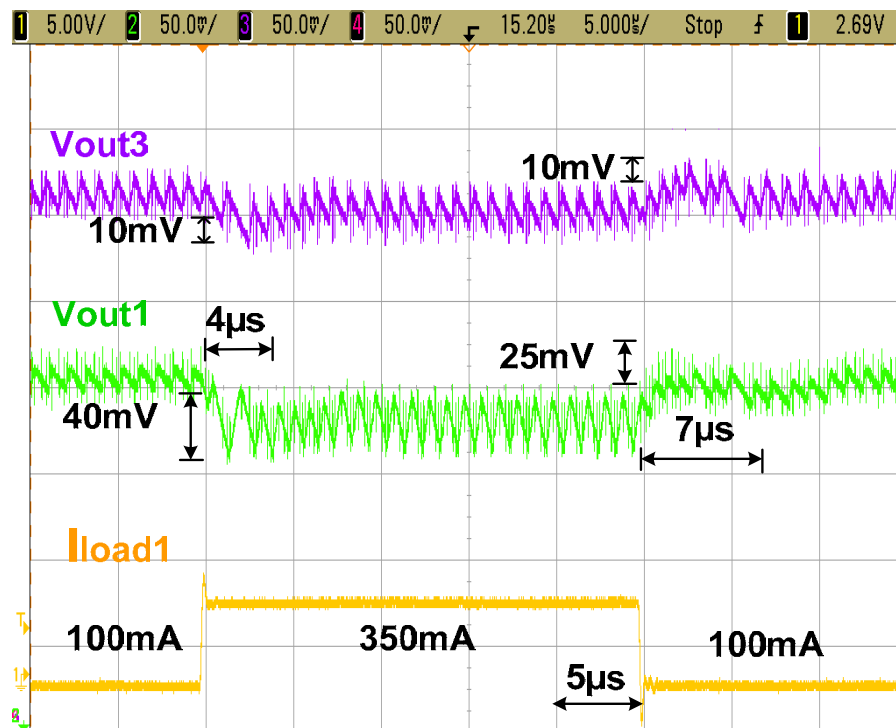
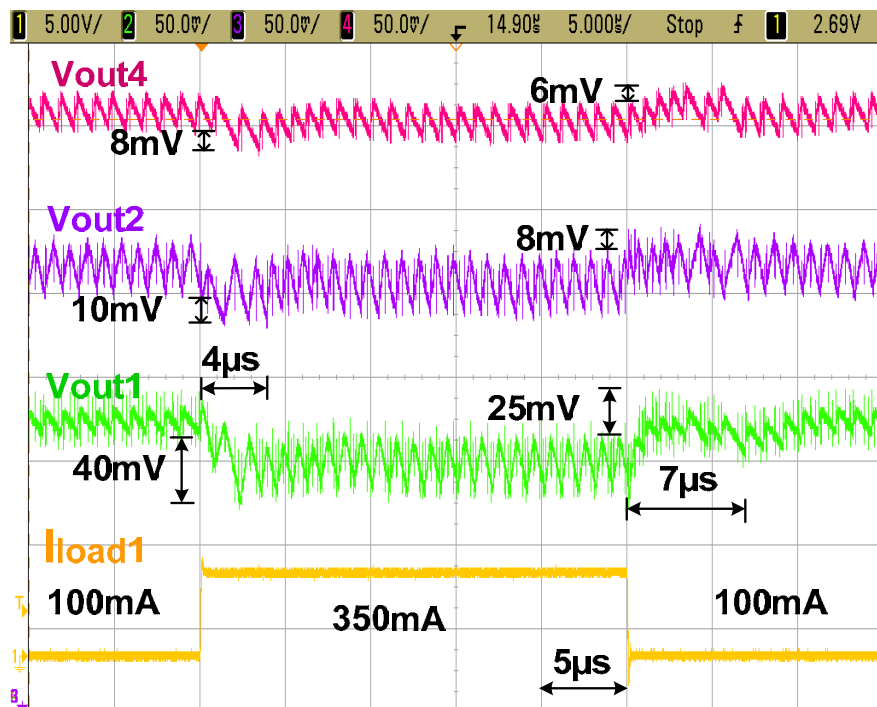


$$V_{out1}=1.5V \quad V_{out2}=0.9V \quad V_{out3}=1.2V \quad V_{out4}=0.6V$$



$$V_{out1}=1.8V \quad V_{out2}=1.5V \quad V_{out3}=1.2V \quad V_{out4}=0.9V$$

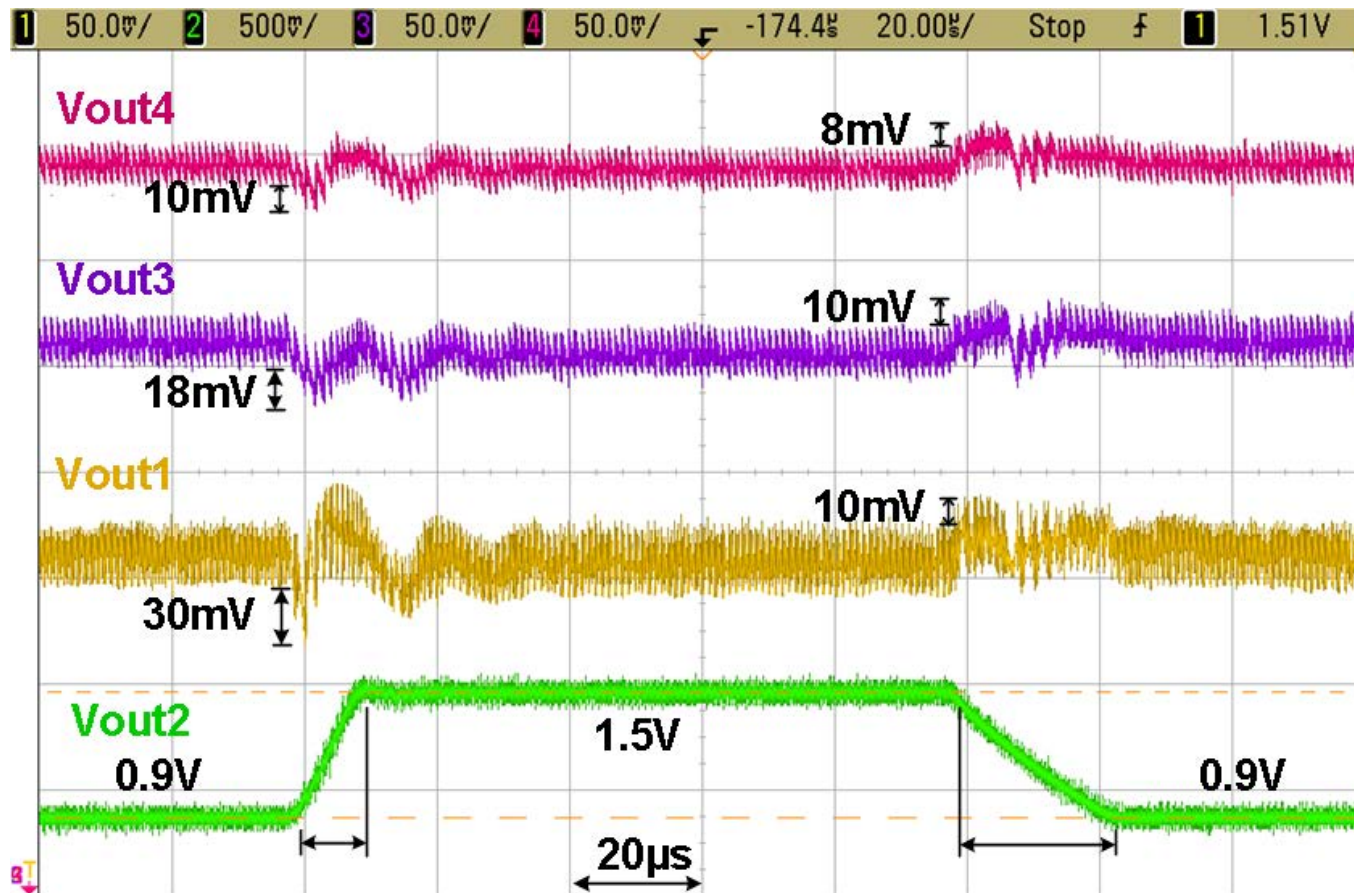
Load-transient response



$$V_g=3.6V \quad V_{out1}=1.8V \quad V_{out2}=1.5V \quad V_{out3}=1.2V \quad V_{out4}=0.9V,$$

$$I_{load1}=100mA \rightarrow 350mA$$

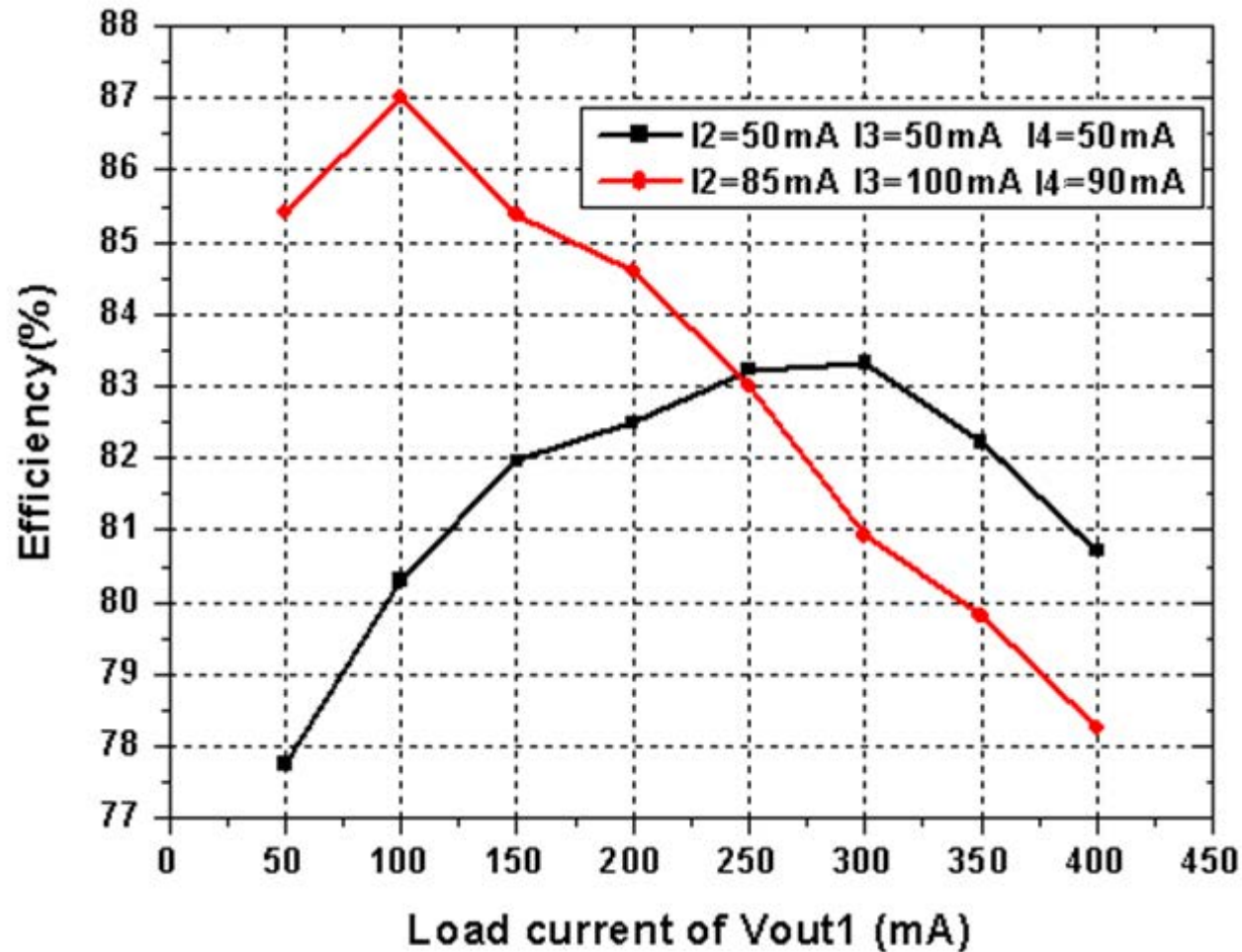
Dynamic voltage scaling



$$V_g = 3.6V \quad V_{out1} = 1.8V \quad V_{out2} = 0.9V \rightarrow 1.5V$$

$$V_{out3} = 1.2V \quad V_{out4} = 0.9V$$

Efficiency



$V_g=3.6V$, $V_{out1}=1.8V$ $V_{out2}=1.5V$ $V_{out3}=1.2V$ $V_{out4}=0.9V$

Summary and Comparison

	[2]	[3]	[4]	This work
Control method	PWM loop control	Comparator control	Charge control	RBAOT control
Topology	4 buck outputs	6 buck outputs	5 buck outputs	4 buck outputs
Supply voltage (V)	2.3~3.6	5.0	3.4~4.3	2.7~5.0
Frequency (MHz)	3	2	1.2	1
Inductor & Capacitor	4.7 μ H & 10 μ F	4.7 μ H & 10 μ F	2.2 μ H & 4.7 μ F	4.7μH & 10μF
Output ripple (mV)	<80	<25*	<40	<30
Load transient (mV/mA)	0.82	0.93	0.6	0.16
Cross regulation (mV/mA)	0.41	0.31	0.067	0.04
Max. Efficiency (%)	no	N/A	83.1	87
Max. Output power(W)	82	1.2	2.232	2.16

* ripple without spike

Reference

- [1] D. Ma, W-H. Ki and C-Y. Tsui, “A Pseudo-CCM/DCM SIMO Switching Converter with Freewheel Switching,” *ISSCC Dig. Tech. Papers*, pp. 390-391, February 2002.
- [2] M. Belloni, E. Bonizzoni, E. Kiseliovas, et al., “A 4-Output Single-Inductor DCDC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current,” *ISSCC Dig. Tech. Papers*, pp. 444-445, February 2008.
- [3] K-C. Lee, C-S.Chae, G-H.Cho, et al., “A PLL-Based High-Stability Single-Inductor 6-channel Output DC-DC Buck Converter,” *ISSCC Dig. Tech. Papers*, pp. 200-201, February 2010.
- [4] C-W. Kuanand and H-C. Lin, “Near-independently regulated 5-output single-inductor DC-DC buck converter delivering 1.2W/mm² in 65nm CMOS,” *ISSCC Dig. Tech. Papers*, pp.274-276, February 2012.

Thank you !

Q & A



Paper 4.4

A 10/30MHz Wide-Duty-Cycle-Range Buck Converter with DDA-Based Type-III Compensator and Fast Reference-Tracking Responses for DVS Applications

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Integrated Power Electronics Laboratory (IPEL)

The Hong Kong University of Science and Technology



香港科技大學

**THE HONG KONG UNIVERSITY OF
SCIENCE AND TECHNOLOGY**

Outline


- ❑ Background
- ❑ High-Accuracy Delay-Compensated Ramp Generator
- ❑ DDA-Based Type-III Compensator
 - ✓ Area-efficient with simple implementation
 - ✓ Fast reference-tracking scheme
- ❑ Measurement Results
- ❑ Conclusions

Dynamic Voltage Scaling (DVS)

- **An effective system technique** to reduce the power consumption in digital systems

$$P = C_{tot} V_{DD}^2 f$$

Vary V_{DD} based on the **loading** conditions



Dynamic Voltage Scaling (DVS)

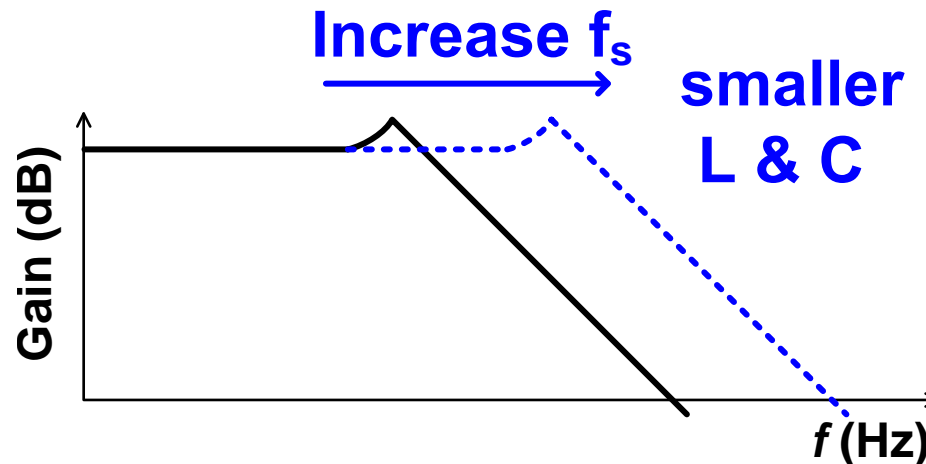
- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency
 - ✓ Fast tracking speed
 - ✓ Wide output range

Dynamic Voltage Scaling (DVS)

- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed
 - ✓ Wide output range

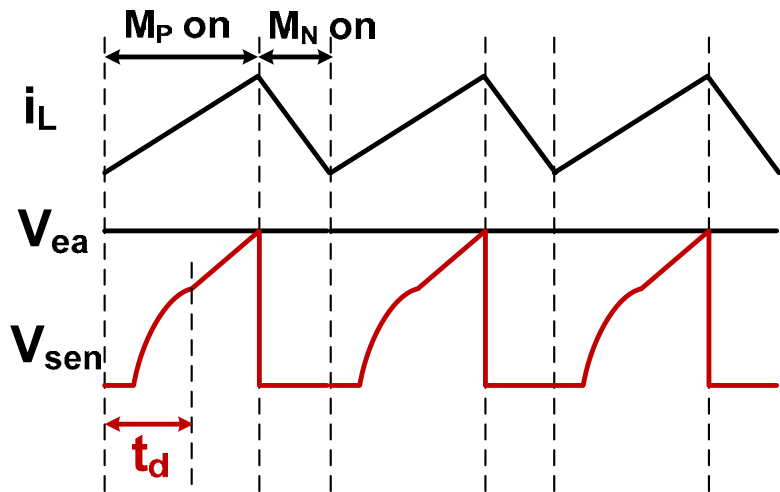
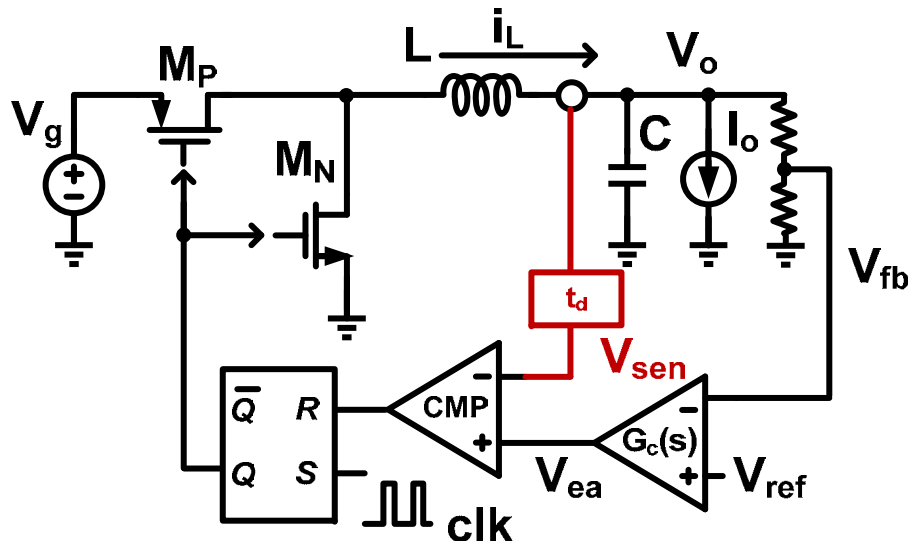
Dynamic Voltage Scaling (DVS)

- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed → **High switching frequency**
 - ✓ Wide output range



Dynamic Voltage Scaling (DVS)

- ❑ **An effective system technique to reduce the power consumption in digital systems**
- ❑ **Requirements on DC-DC converters**
 - ✓ **High efficiency** → **Inductive switching converters**
 - ✓ **Fast tracking speed** → **High switching frequency**
 - ✓ **Wide output range** → **Current-mode control?**



4.4: A 10/30MHz Wide-Duty-Cycle-Range Buck Converter with DDA-based Type-III Compensator and Fast Reference-Tracking Responses for DVS Applications

Dynamic Voltage Scaling (DVS)

- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed → High switching frequency
 - ✓ Wide output range → **Current-mode control?**

Switching frequency	3.5 MHz	5 MHz
Input voltage range	2.7 V to 4.2 V	
Load current	≤ 500 mA	
Off-chip inductor	1 μH (EPL2014-102ML)	
Off-chip capacitor	4.7 μF (EMK316B7475KL-T)	
Max power efficiency	94%	91%
Duty-ratio range	0.78	0.6

- ***Auto-Selectable Peak- and Valley-Current Control [JSSC 2011]***

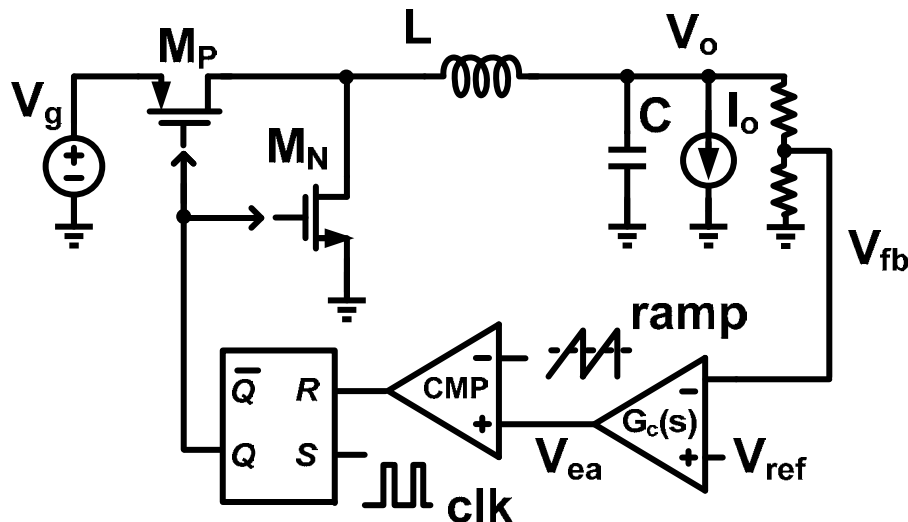
$$f_{sw} = 3.5 \text{ MHz} \rightarrow D_{\max} - D_{\min} = 0.78$$

$$f_{sw} = 5 \text{ MHz} \rightarrow D_{\max} - D_{\min} = 0.6$$

$$\text{Duty-cycle: } D = V_{\text{out}} / V_g$$

Dynamic Voltage Scaling (DVS)

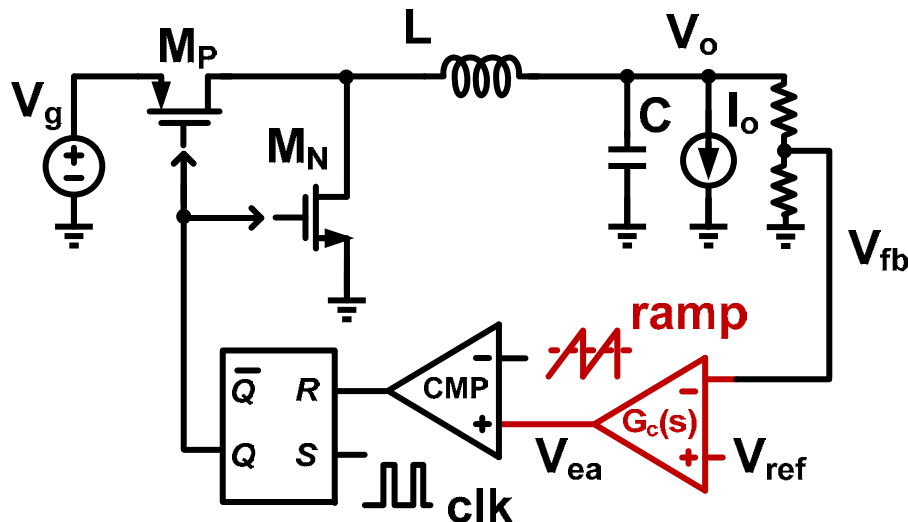
- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed → High switching frequency
 - ✓ Wide output range → Voltage-mode control



4.4: A 10/30MHz Wide-Duty-Cycle-Range Buck Converter with DDA-based Type-III Compensator and Fast Reference-Tracking Responses for DVS Applications

Dynamic Voltage Scaling (DVS)

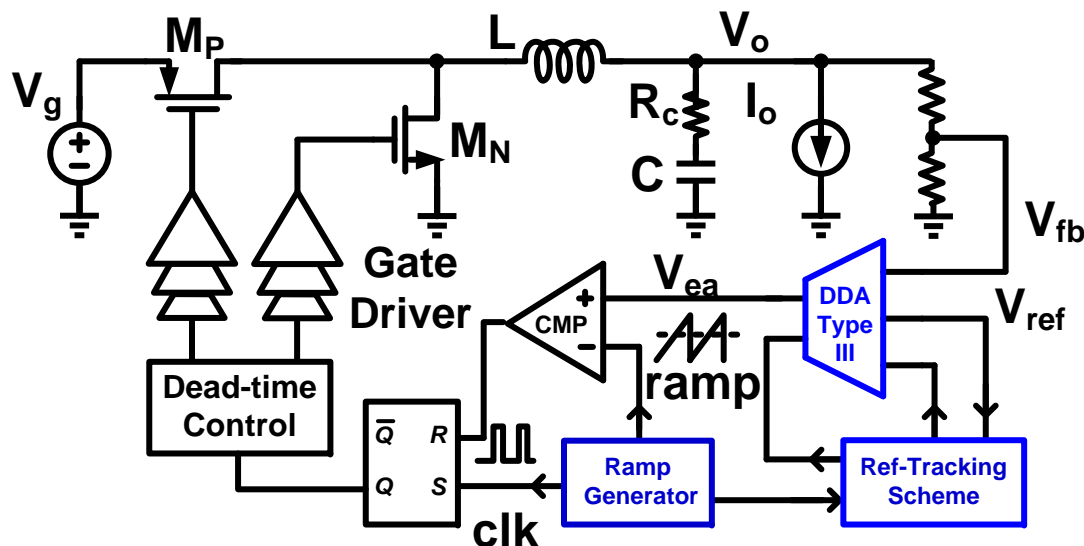
- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed → High switching frequency
 - ✓ Wide output range → Voltage-mode control



× Type-III Compensator
× Ramp Generator

Dynamic Voltage Scaling (DVS)

- ❑ An effective system technique to reduce the power consumption in digital systems
- ❑ Requirements on DC-DC converters
 - ✓ High efficiency → Inductive switching converters
 - ✓ Fast tracking speed → High switching frequency
 - ✓ Wide output range → Voltage-mode control



- ✓ High-accuracy delay compensated ramp generator
- ✓ Area-efficient Type-III compensator
- ✓ Fast tracking scheme

4.4: A 10/30MHz Wide-Duty-Cycle-Range Buck Converter with DDA-based Type-III Compensator and Fast Reference-Tracking Responses for DVS Applications

Outline

- Background

- **High-Accuracy Delay-Compensated Ramp Generator**

- DDA-Based Type-III Compensator

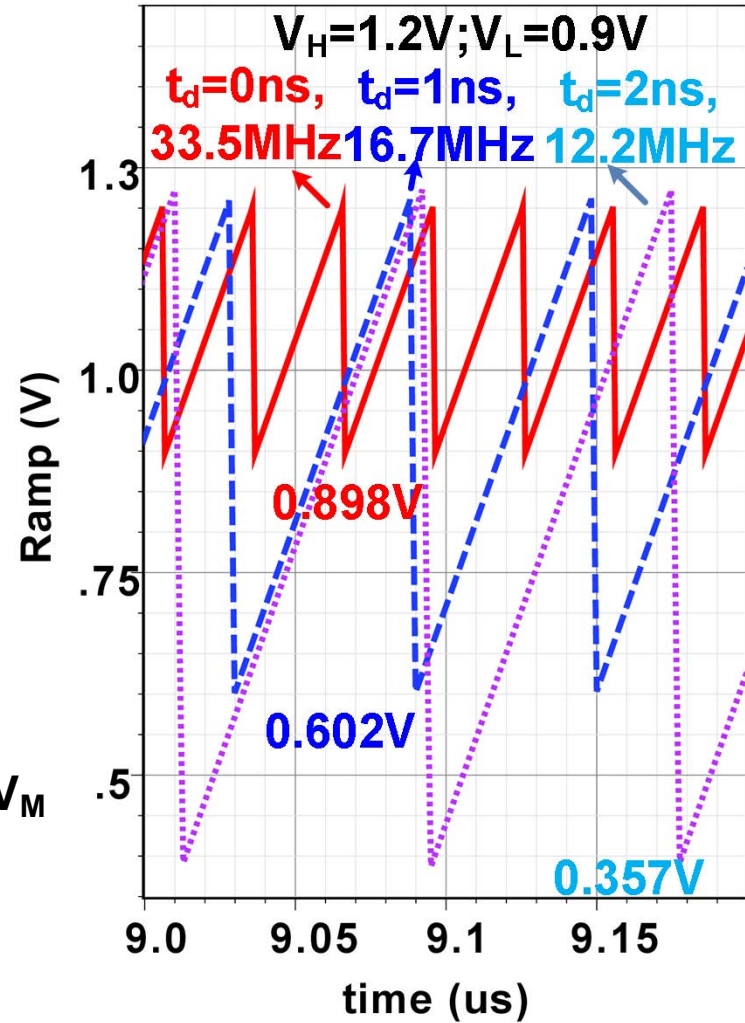
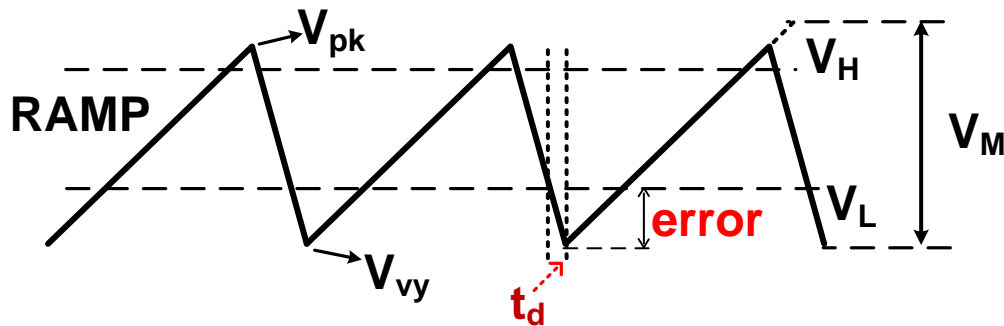
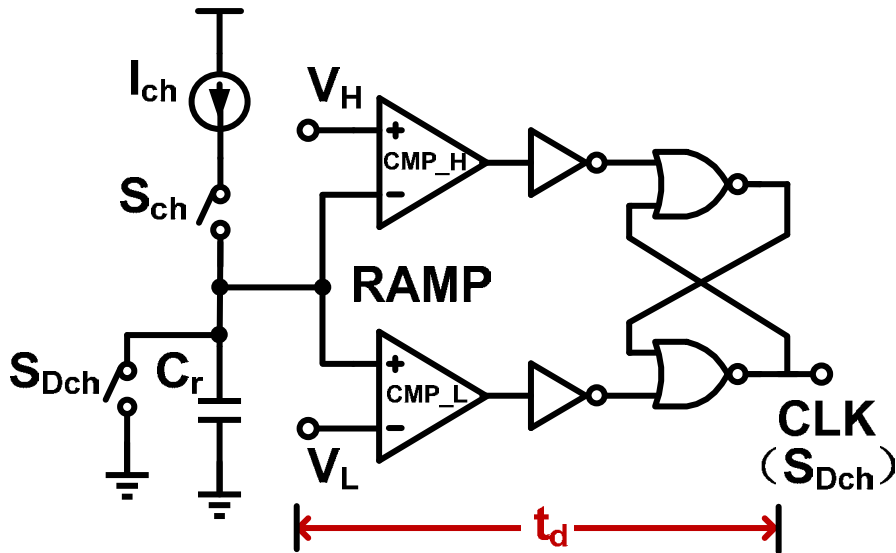
 - ✓ Area-efficient with simple implementation

 - ✓ Fast reference-tracking scheme

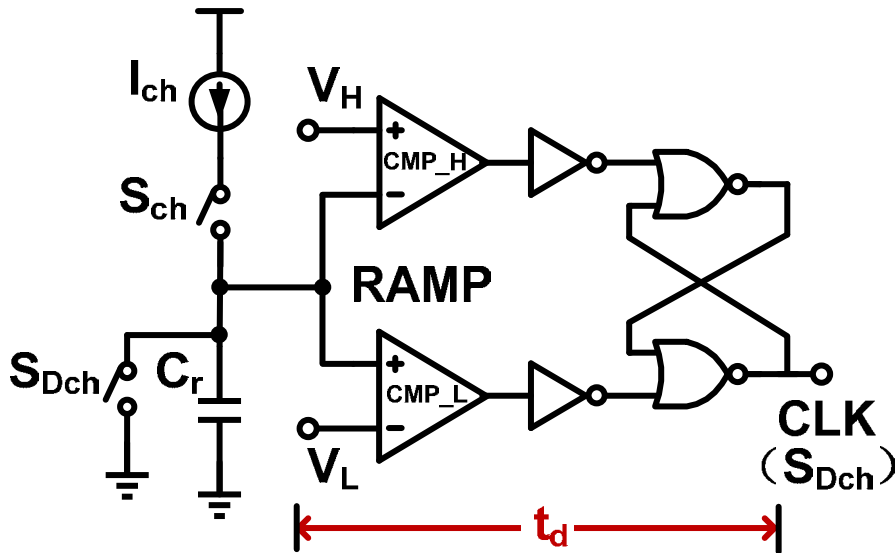
- Measurement Results

- Conclusions

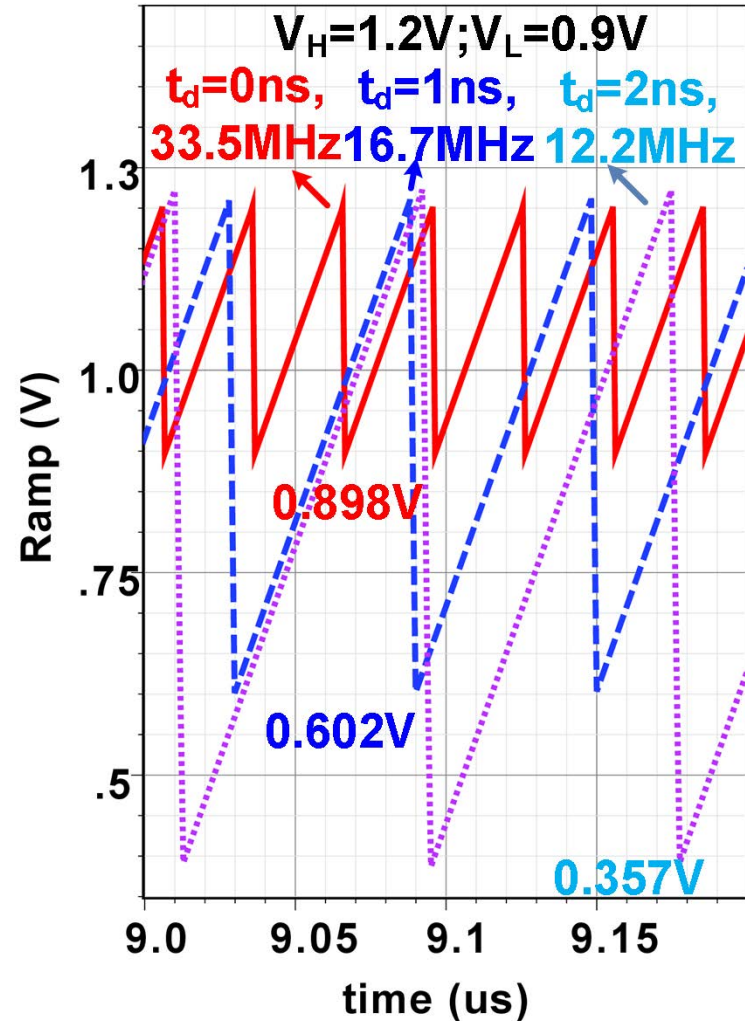
Conventional Ramp Generator



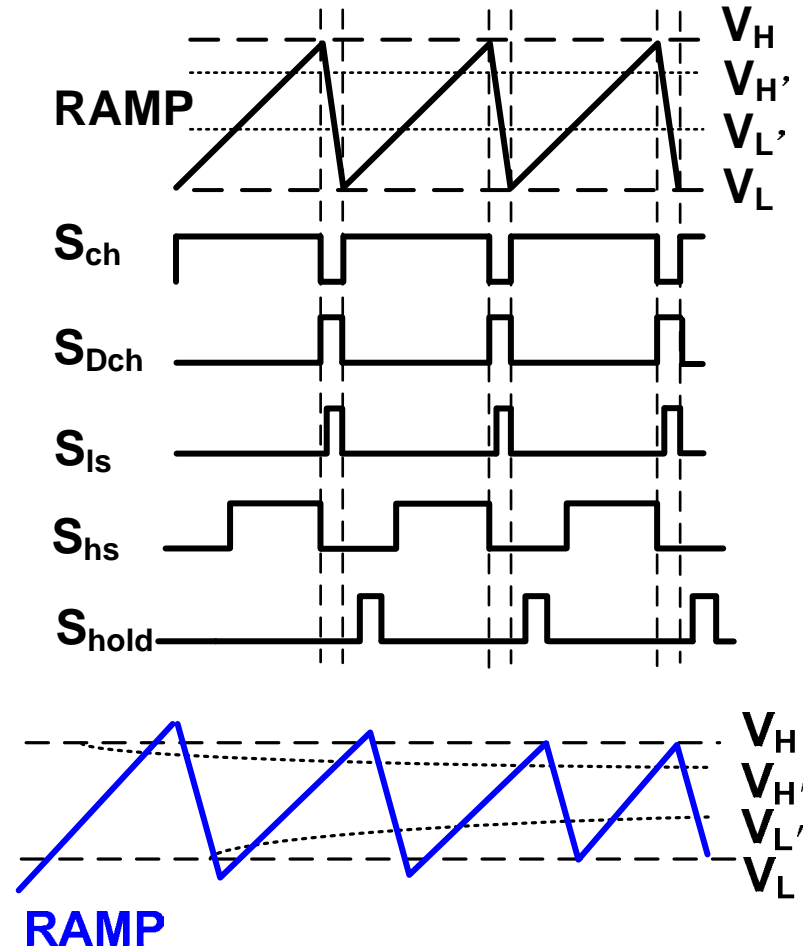
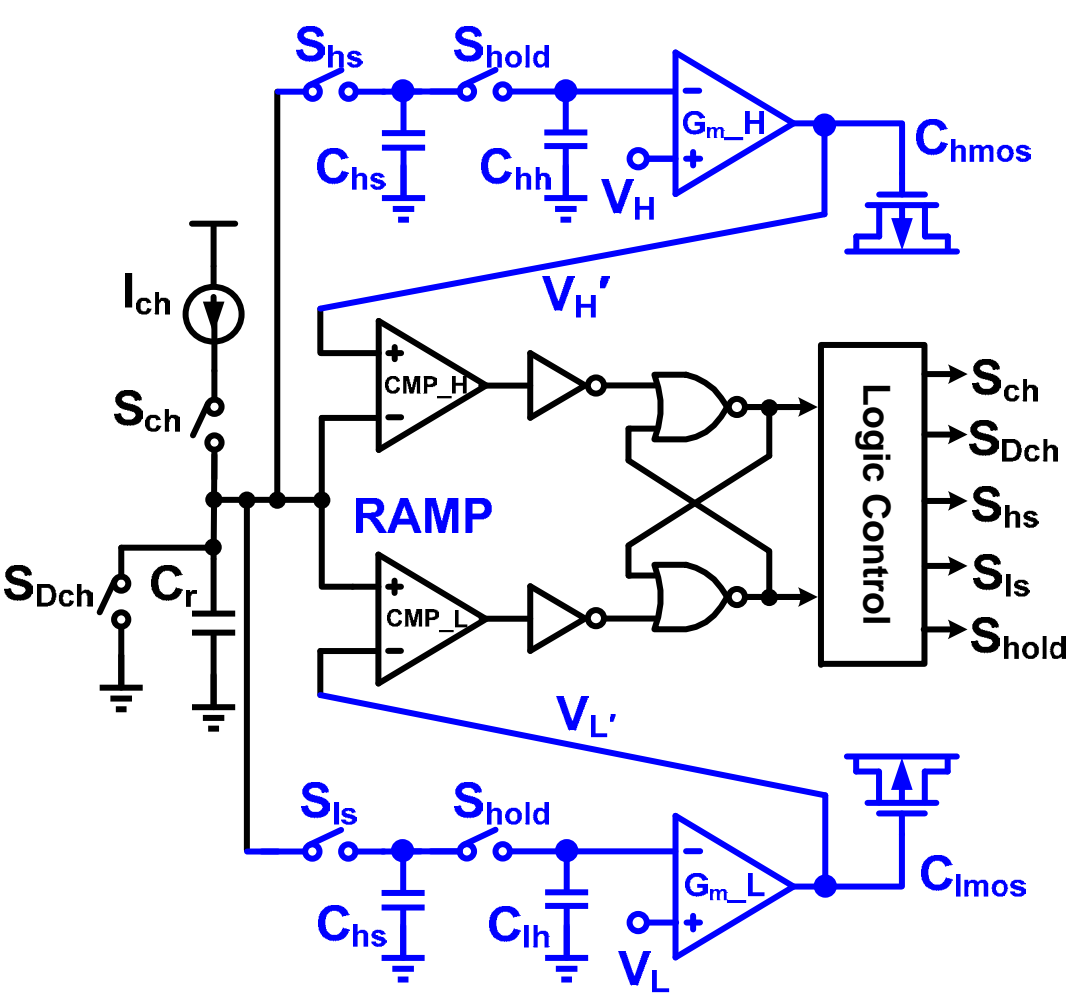
Conventional Ramp Generator



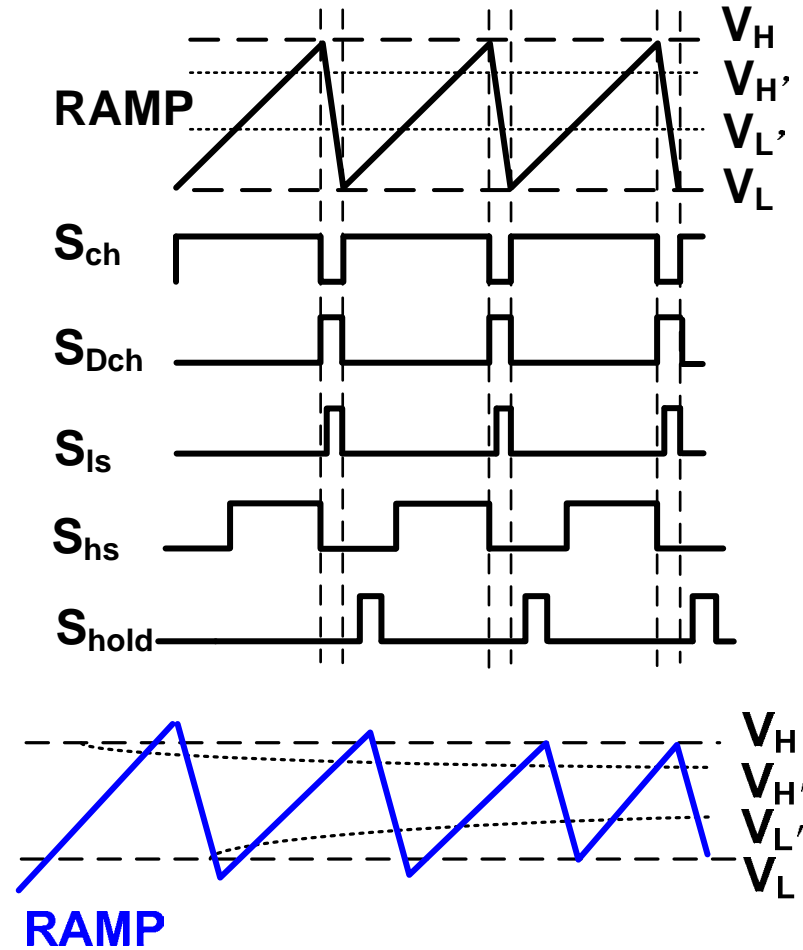
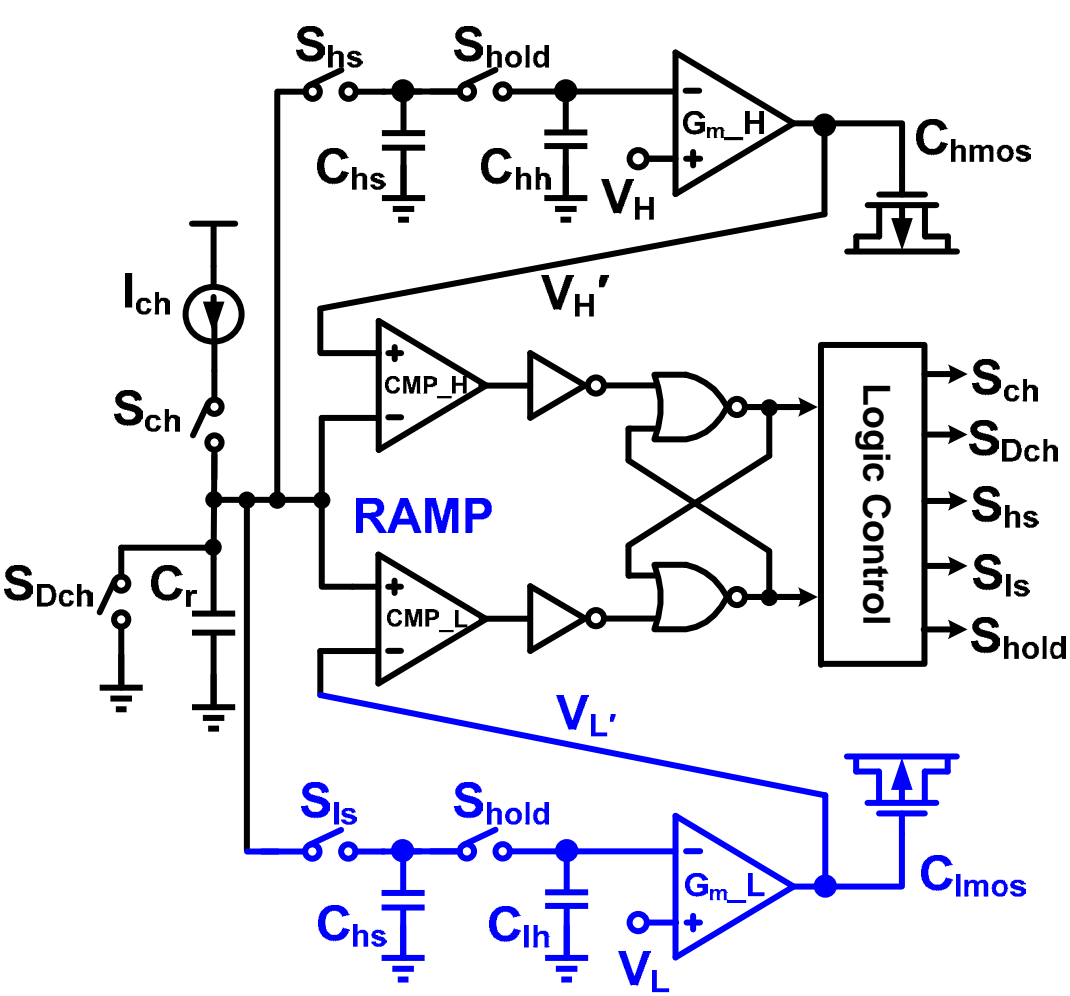
- ❑ High speed comparator
- x Power hungry
- x Difficult to design
- ❑ PVT variations



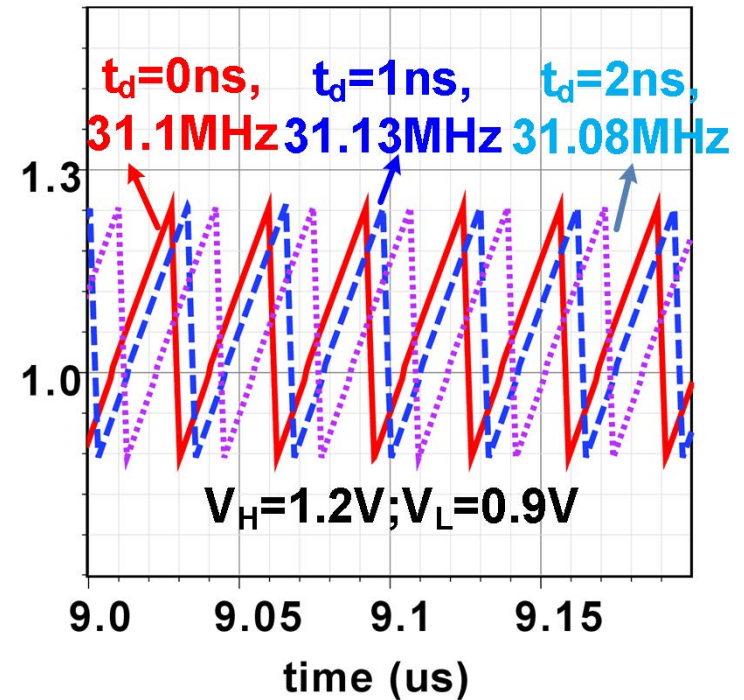
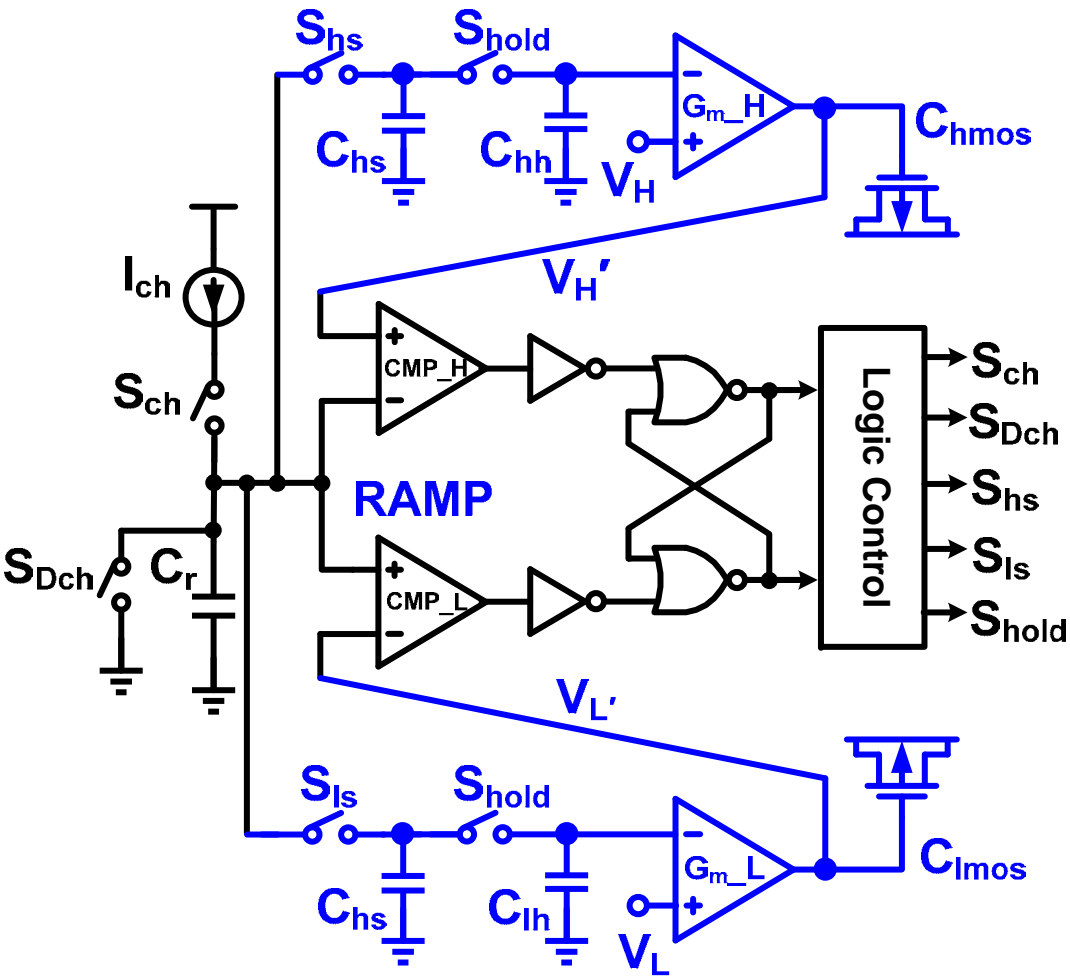
Proposed Ramp Generator



Proposed Ramp Generator



Proposed Ramp Generator

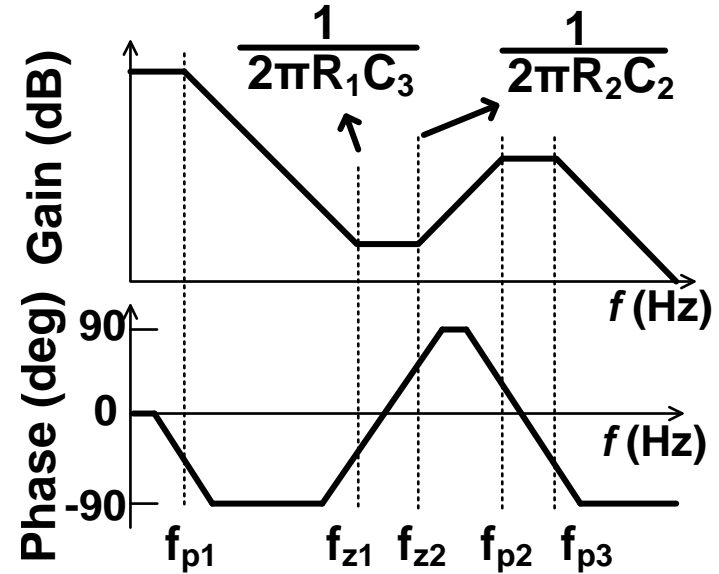
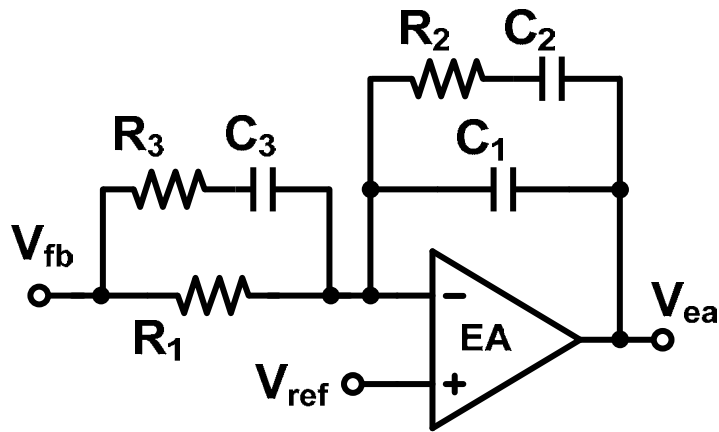


- ✓ High-Accuracy
- ✓ Power-Efficient

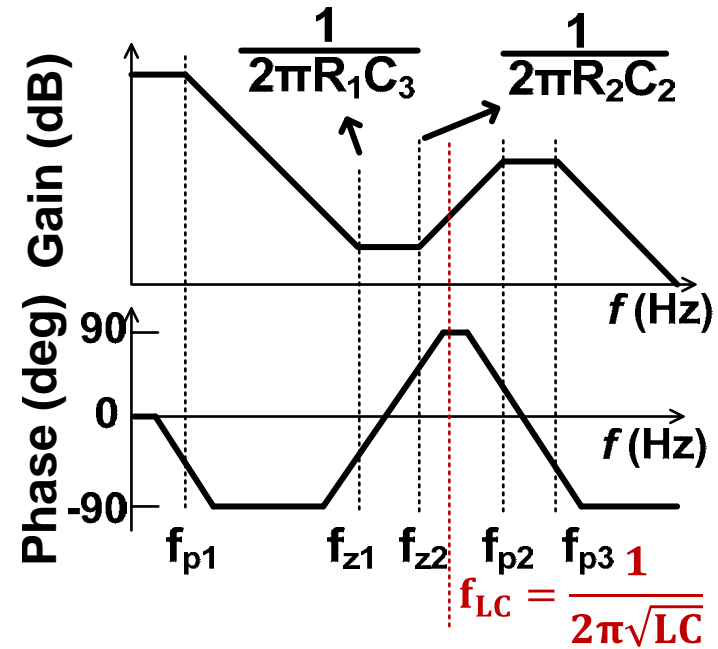
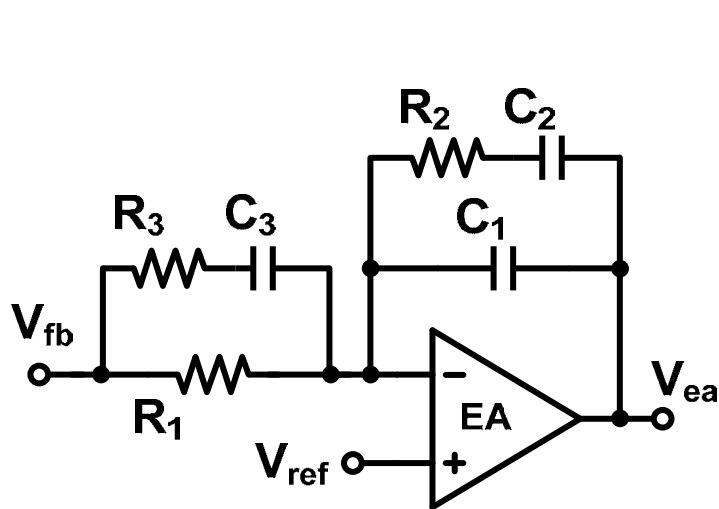
Outline

- Background
- High-Accuracy Delay-Compensated Ramp Generator
- **DDA-Based Type-III Compensator**
 - ✓ **Area-efficient with simple implementation**
 - ✓ Fast reference-tracking scheme
- Measurement Results
- Conclusions

Conventional Type-III Compensator



Conventional Type-III Compensator



□ Example:

$$\begin{aligned} f_{sw} &= 10\text{MHz} \\ L &= 0.33\mu\text{H} \\ C &= 3.3\mu\text{F} \end{aligned}$$

$$\begin{aligned} f_{z1} &= 0.25f_{LC} \\ f_{z2} &= f_{LC} \end{aligned}$$

$$\begin{aligned} R_1 &= R_2 = 200\text{k}\Omega \\ C_2/C_3 &= 5\text{pF}/20\text{pF} \end{aligned}$$

✓ Fast Response

✗ Area Consuming

Pseudo Type-III Compensator [JSSC 2010]

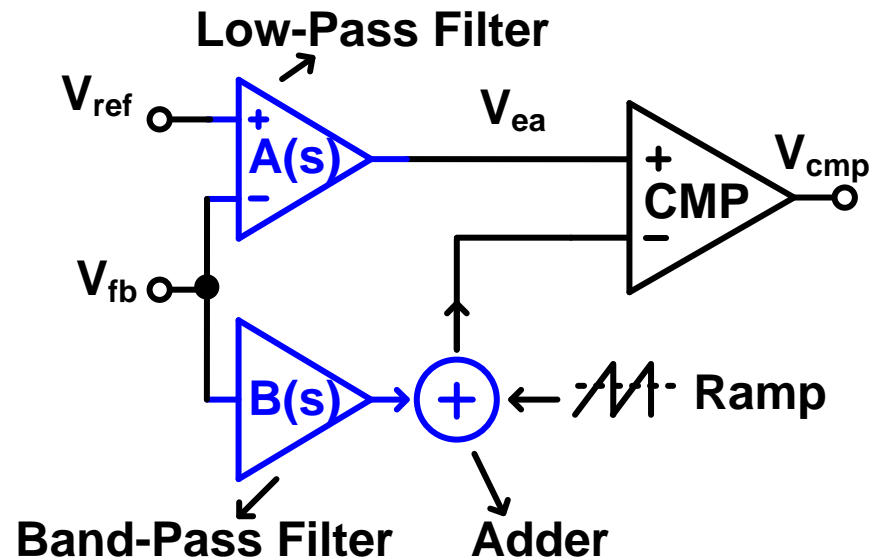
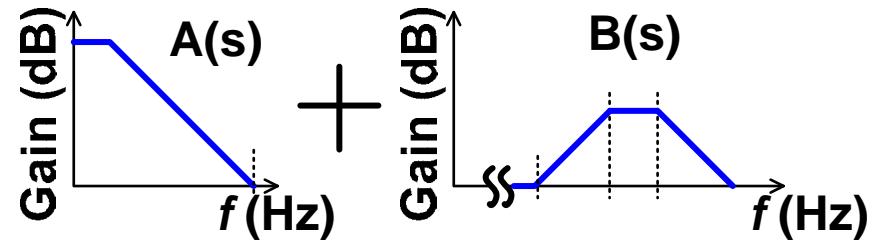
$$A(s) = \frac{G_{ea}}{1 + s/p_0} ;$$

$$B(s) = \frac{G_{bpf}(1 + s/z_0)}{(1 + s/p_1)(1 + s/p_2)}$$

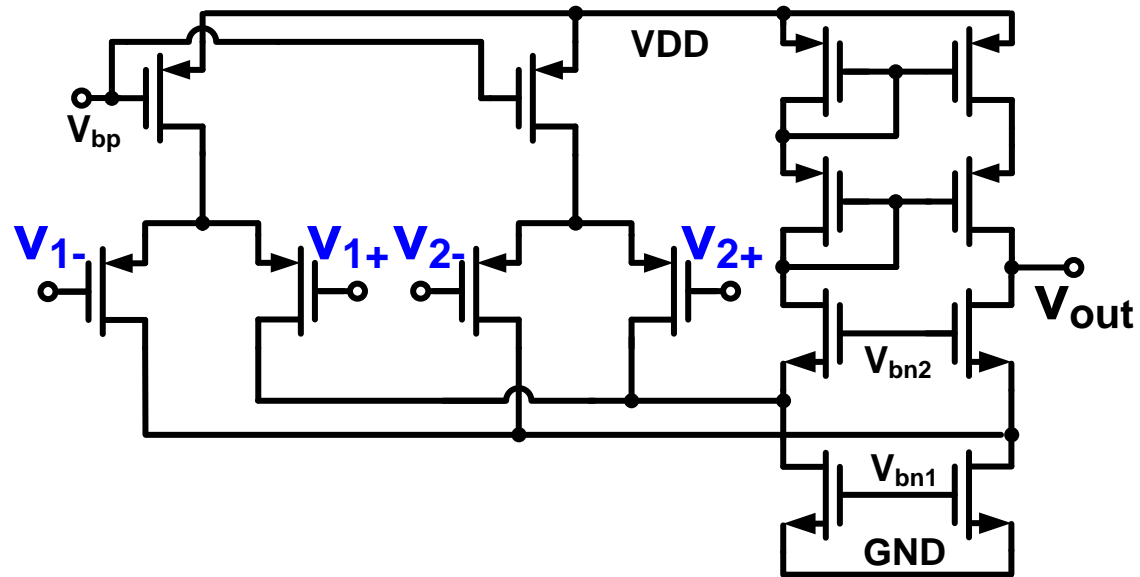
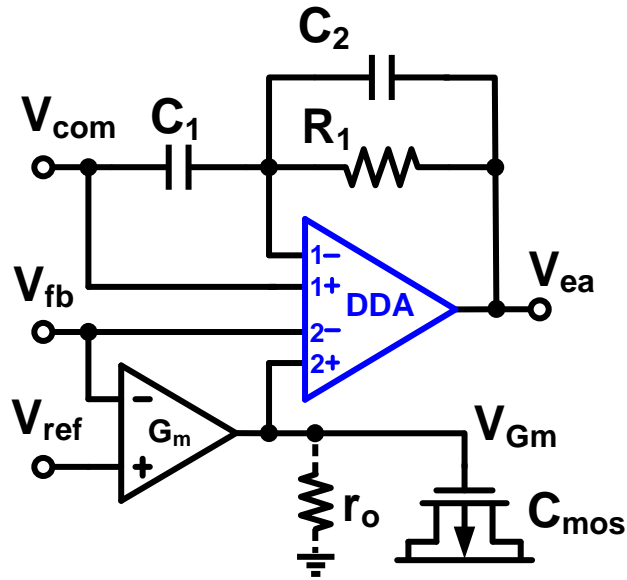
$$z_{1,2} = \frac{z_0}{2} \left(1 \pm \sqrt{1 - \frac{4G_{ea}p_0}{z_0}} \right)$$

✓ **Area-Efficient**

✗ **Complicated Implementation**

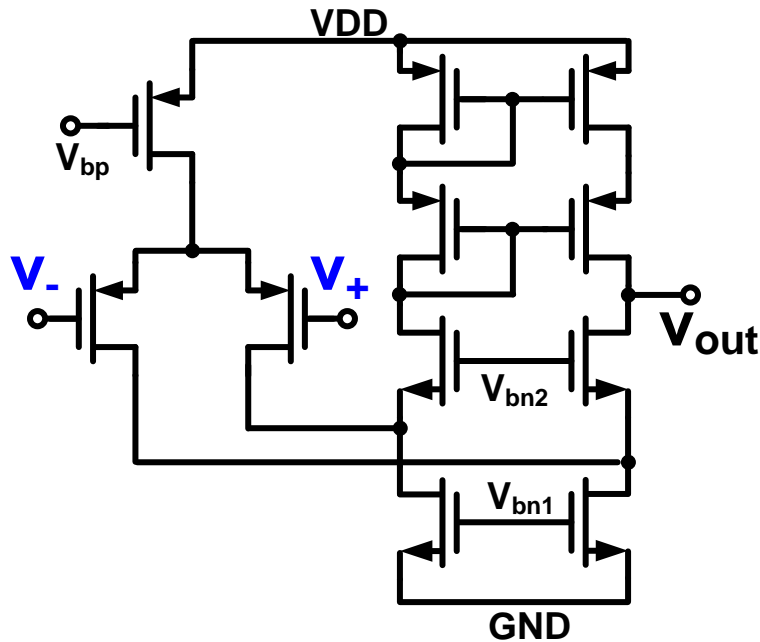


Proposed Type-III Compensator

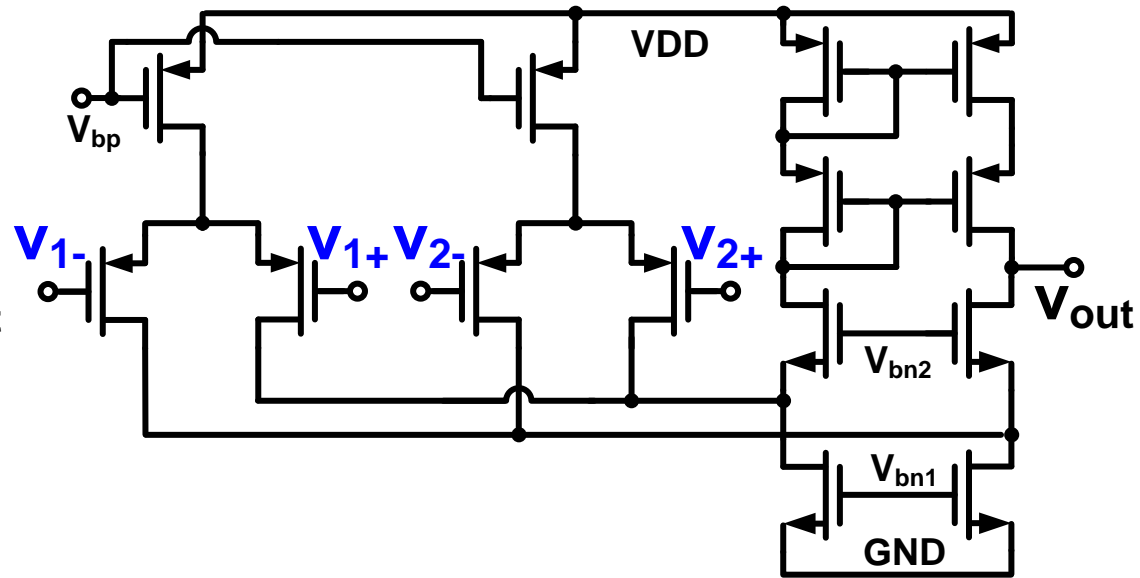


Differential Difference Amplifier (DDA) [JSSC 1987]

Differential Difference Amplifier (DDA)



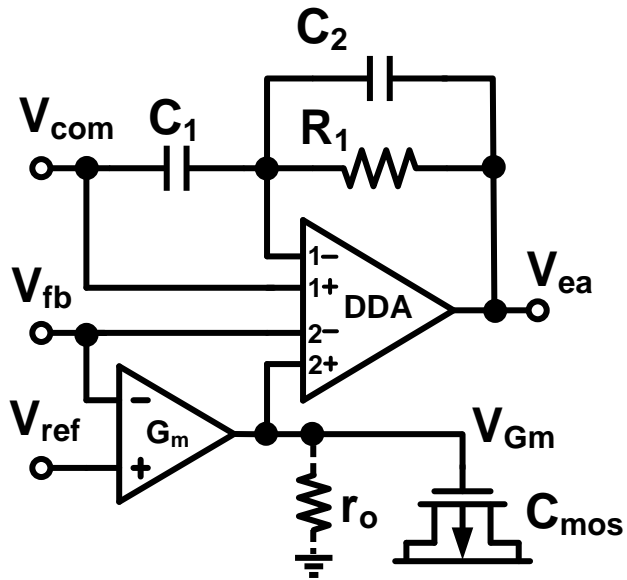
$$V_+ = V_-$$



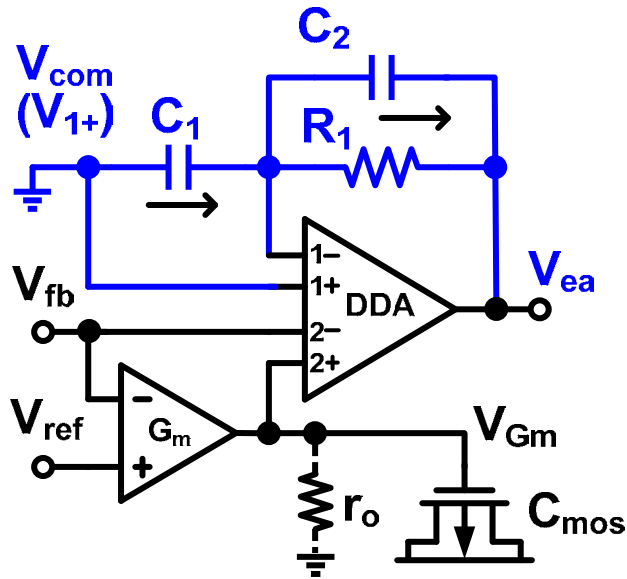
$$V_{1+} + V_{2+} = V_{1-} + V_{2-}$$

$$\Rightarrow V_{1+} - V_{1-} = -(V_{2+} - V_{2-})$$

DDA-Based Type-III Compensator



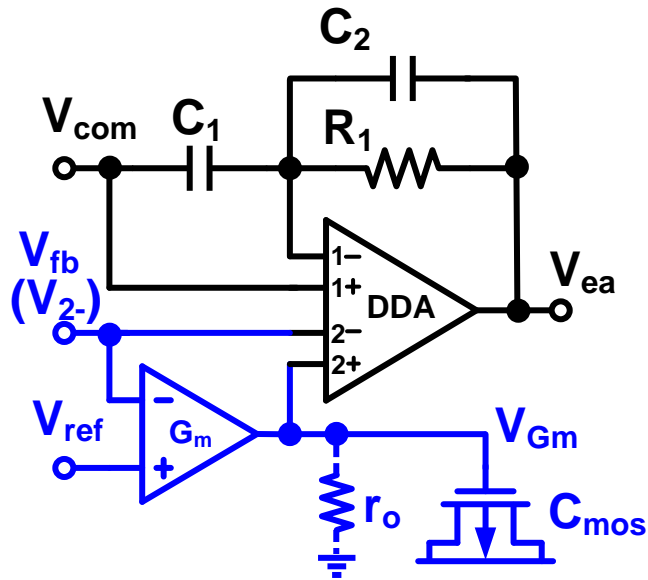
DDA-Based Type-III Compensator



$$sC_1(V_{1+} - V_{1-}) = \left(sC_2 + \frac{1}{R_1} \right) (V_{1-} - V_{ea})$$

$$\Rightarrow V_{ea} = -\frac{1 + s(C_1 + C_2)R_1}{1 + sC_2R_1} (V_{1+} - V_{1-})$$

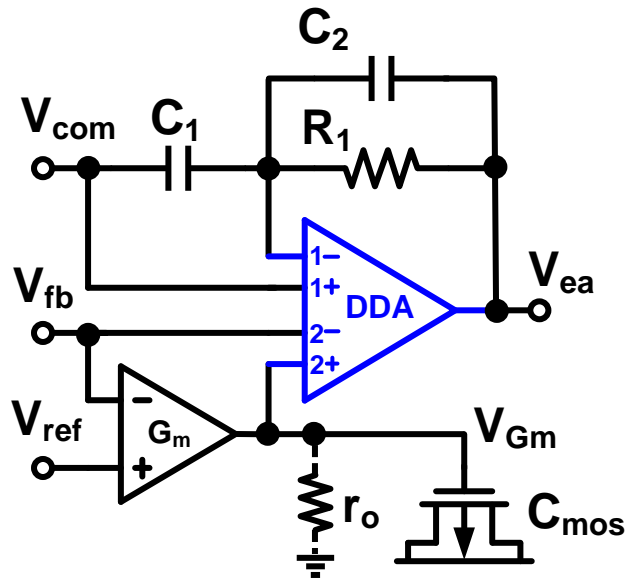
DDA-Based Type-III Compensator



$$V_{ea} = - \frac{1 + s(C_1 + C_2)R_1}{1 + sC_2R_1} (V_{1+} - V_{1-})$$

$$V_{2+} - V_{2-} = V_{fb} \left(- \frac{G_m r_o}{1 + sC_{mos}r_o} - 1 \right)$$

DDA-Based Type-III Compensator

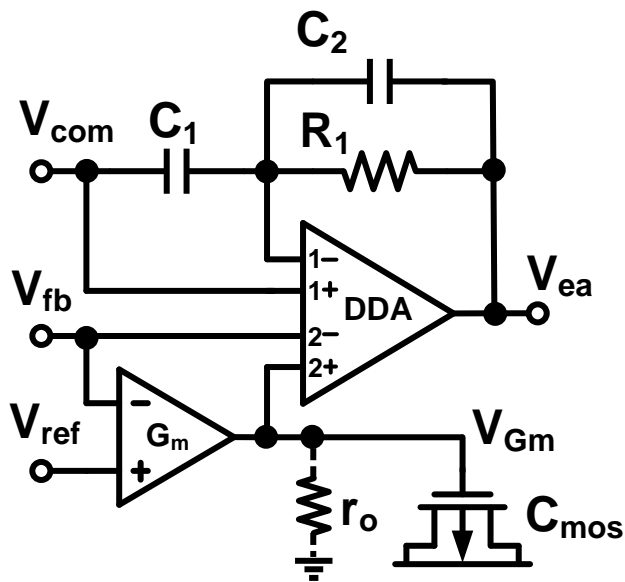


$$V_{ea} = -\frac{1 + s(C_1 + C_2)R_1}{1 + sC_2R_1} (V_{1+} - V_{1-})$$

$$V_{2+} - V_{2-} = V_{fb} \left(-\frac{G_m r_o}{1 + sC_{mos}r_o} - 1 \right)$$

$$V_{1+} - V_{1-} = -(V_{2+} - V_{2-})$$

DDA-Based Type-III Compensator



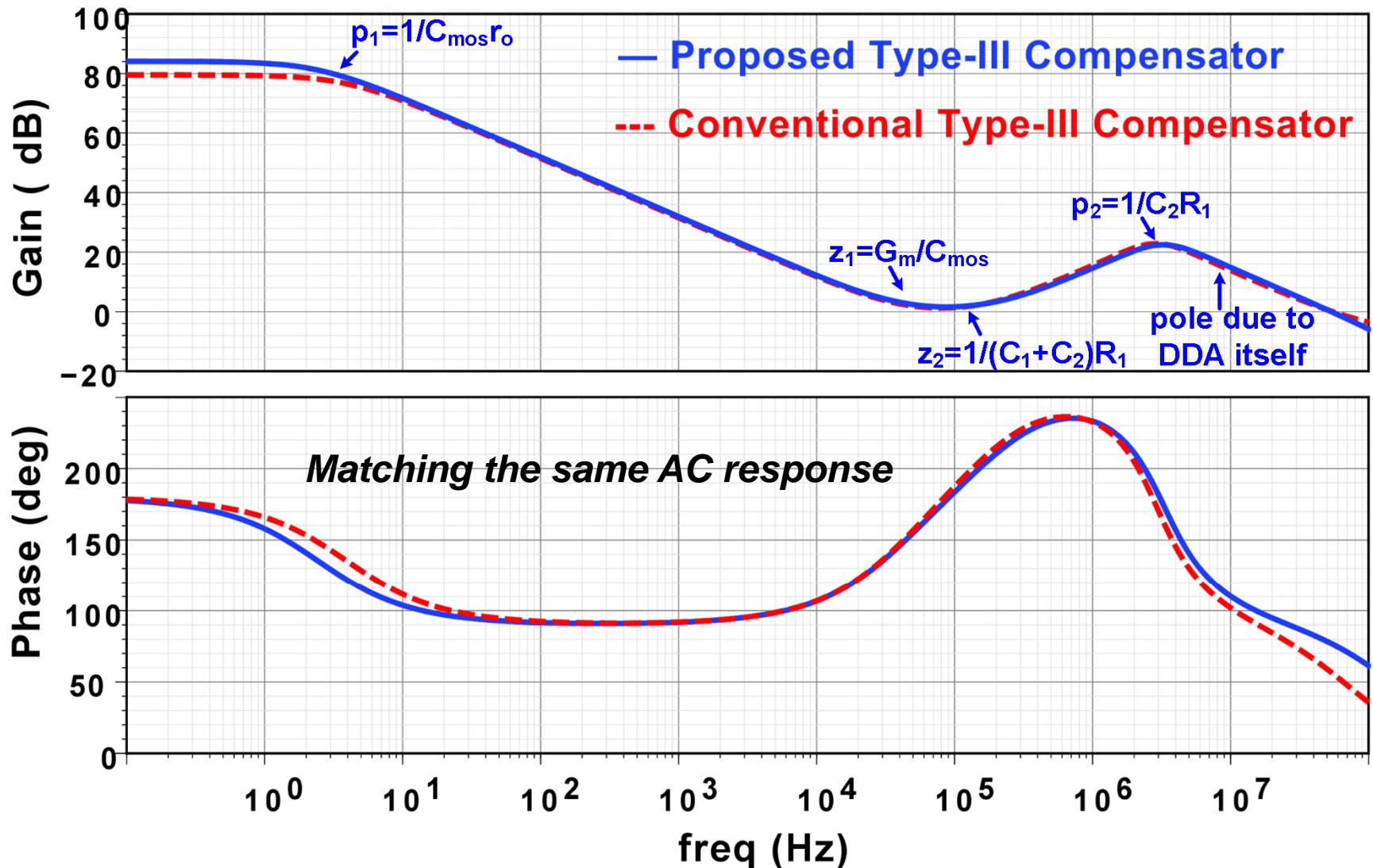
$$\left\{ \begin{array}{l} V_{ea} = -\frac{1 + s(C_1 + C_2)R_1}{1 + sC_2R_1}(V_{1+} - V_{1-}) \\ V_{2+} - V_{2-} = V_{fb} \left(-\frac{G_m r_o}{1 + sC_{mos}r_o} - 1 \right) \\ V_{1+} - V_{1-} = -(V_{2+} - V_{2-}) \end{array} \right.$$

$$\Rightarrow \mathbf{G_c(s)} = \frac{\mathbf{V_{ea}}}{\mathbf{V_{fb}}} = (\mathbf{1 + G_m r_o}) \frac{(\mathbf{1 + sC_{mos}/G_m})(\mathbf{1 + s(C_1 + C_2)R_1})}{(\mathbf{1 + sC_{mos}r_o})(\mathbf{1 + sC_2R_1})}$$

✓ Area-Efficient

✓ Simple Implementation

Comparison

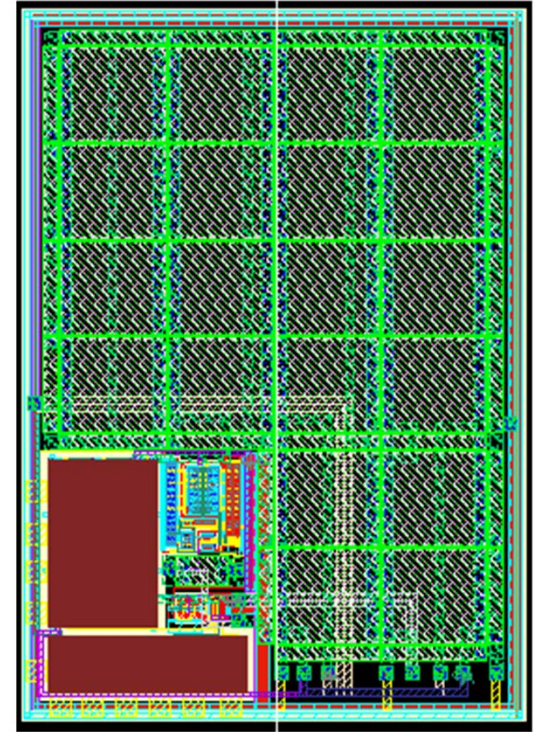


Comparison

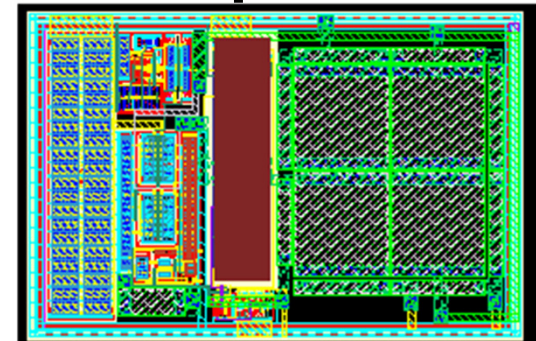
Design	Conventional	Proposed
Capacitor	25pF MIM	5pF MIM 10pF MOS
Resistor	400k Ω	200k Ω
Amplifier	1	2
Area	0.048mm ²	0.019mm ²

60% area-reduction

Conventional



Proposed



Outline

- Background
- High-Accuracy Delay-Compensated Ramp Generator
- **DDA-Based Type-III Compensator**
 - ✓ Area-efficient with simple implementation
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- Measurement Results
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End-Point Prediction (EPP) [TCAS2 2006]

□ A **feedforward** scheme to predict the correct D for CCM

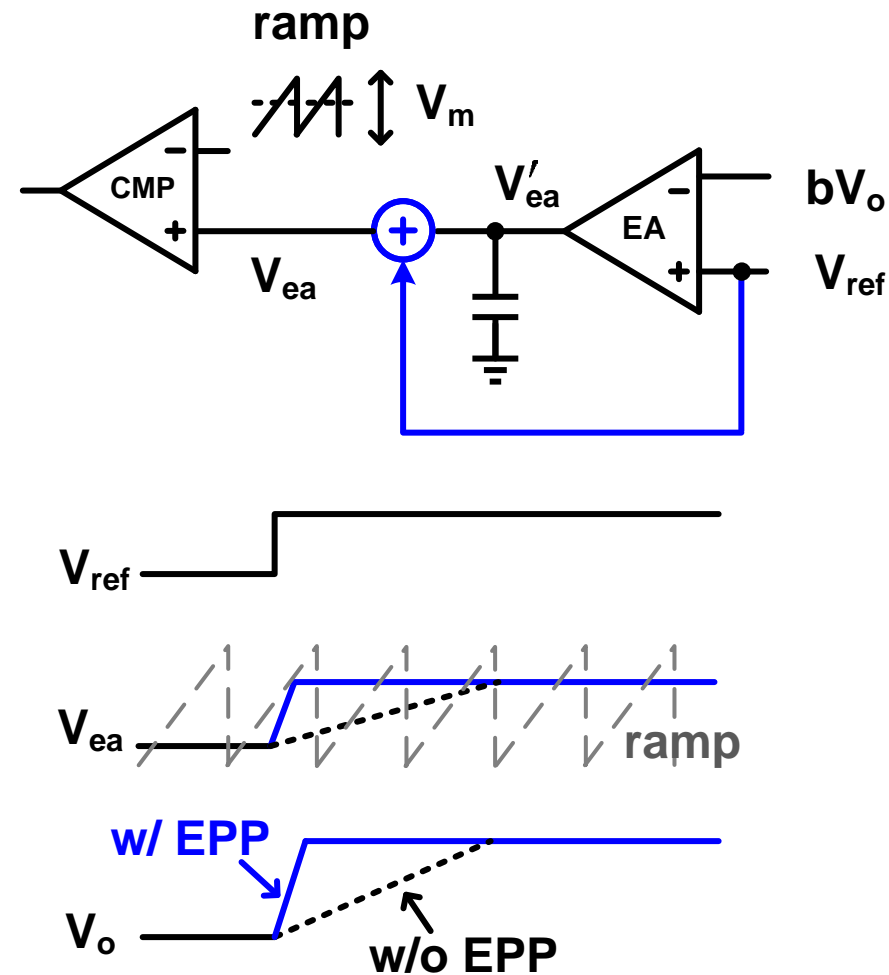
$$D = \frac{V_o}{V_g} = \frac{V_{\text{ref}}/b}{V_g} = \frac{V_{\text{ea}} - V_L}{V_m}$$

$$\Rightarrow V_{\text{ea}} = V_m V_{\text{ref}}/bV_g + V_L$$

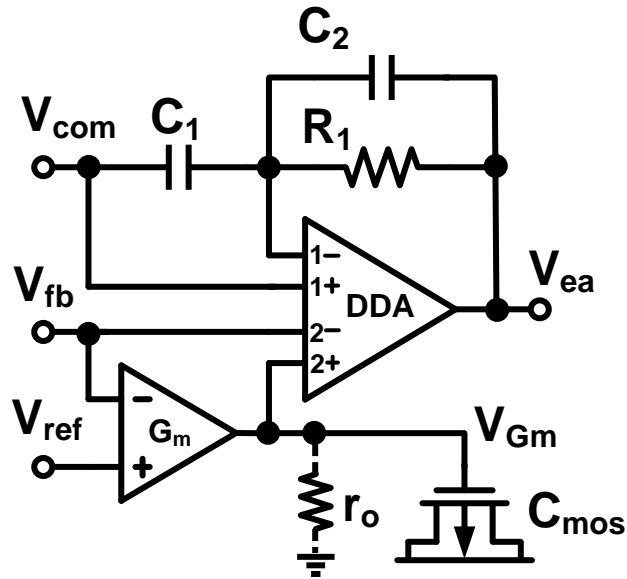
Design:

$$V_m = V_H - V_L = bV_g$$

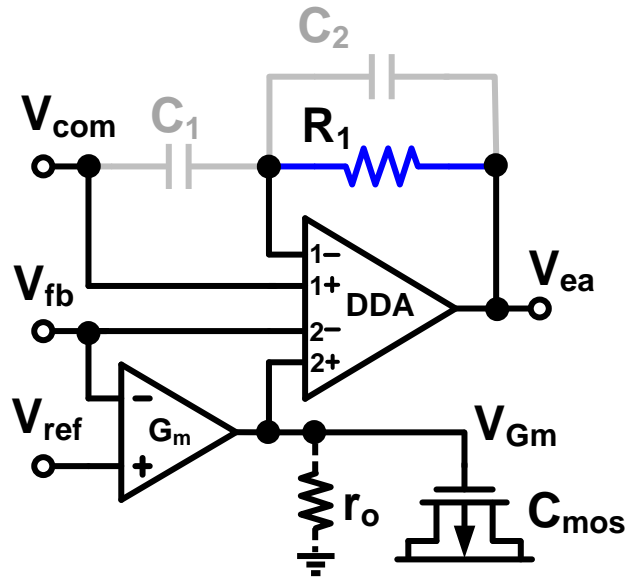
$$\Rightarrow V_{\text{ea}} = V_{\text{ref}} + V_L$$



EPP in DDA-Based Type-III Compensator

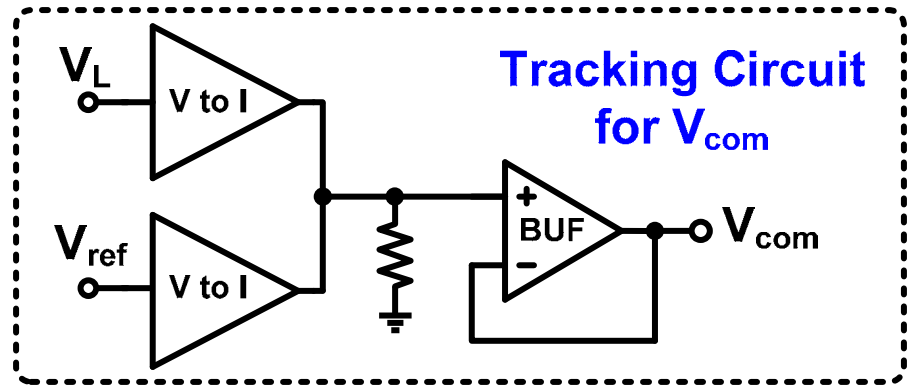
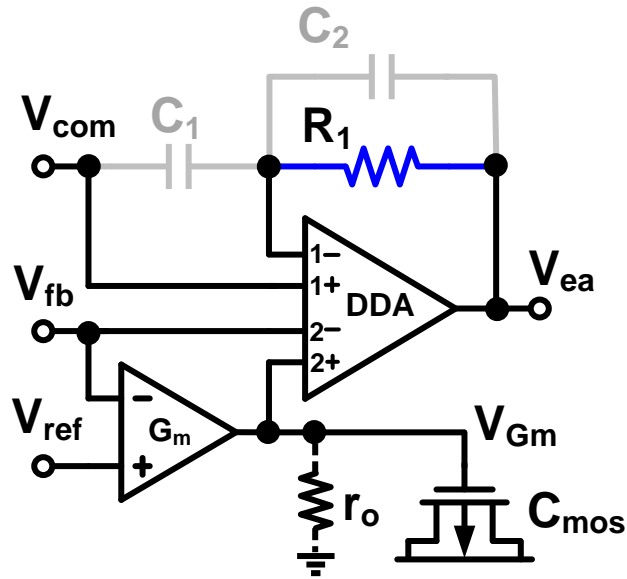


EPP in DDA-Based Type-III Compensator



$$V_{1-} = V_{ea}$$

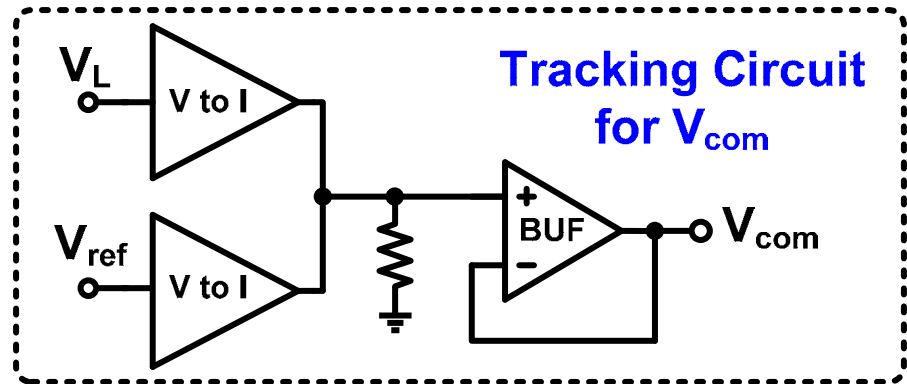
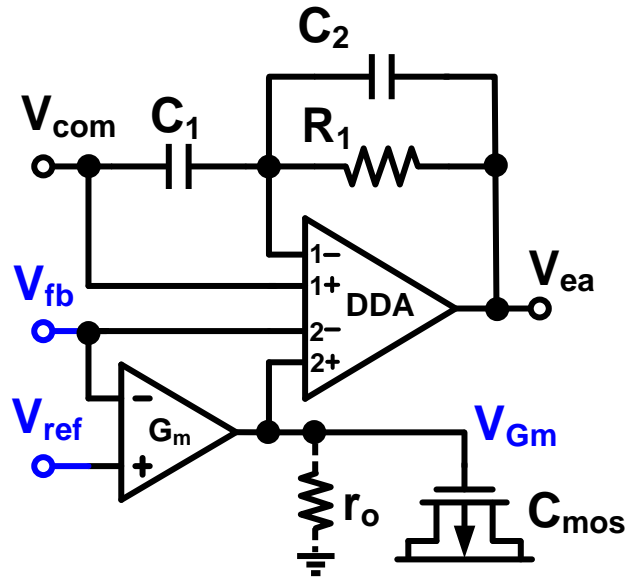
EPP in DDA-Based Type-III Compensator



$$V_{ea} = V_m V_{ref} / b V_g + V_L$$

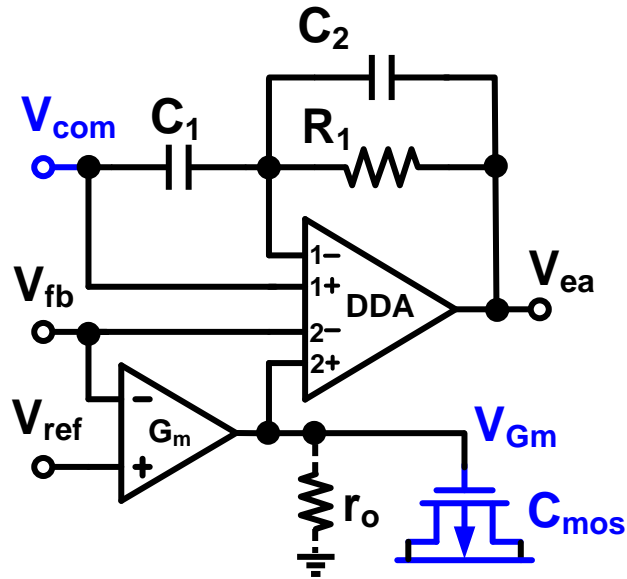
$$\left. \begin{array}{l} V_{1-} = V_{ea} \\ V_{com} = V_{ea} \end{array} \right\} \Rightarrow V_{1+} = V_{1-}$$

EPP in DDA-Based Type-III Compensator



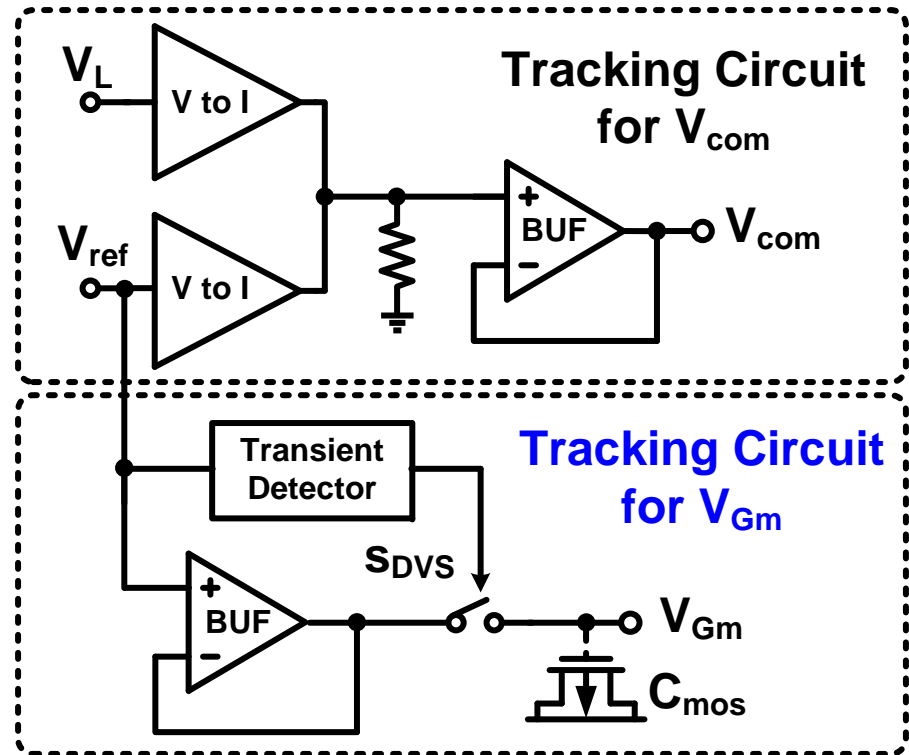
$$\left. \begin{array}{l} V_{1-} = V_{ea} \\ V_{com} = V_{ea} \end{array} \right\} \Rightarrow V_{1+} = V_{1-} \left\{ \begin{array}{l} \Rightarrow V_{2+} = V_{2-} \\ V_{1+} - V_{1-} = -(V_{2+} - V_{2-}) \end{array} \right. \Rightarrow V_{Gm} = V_{ref} = V_{fb}$$

EPP in DDA-Based Type-III Compensator



$$\left. \begin{aligned} V_{1-} &= V_{ea} \\ V_{com} &= V_{ea} \end{aligned} \right\} \Rightarrow V_{1+} = V_{1-}$$

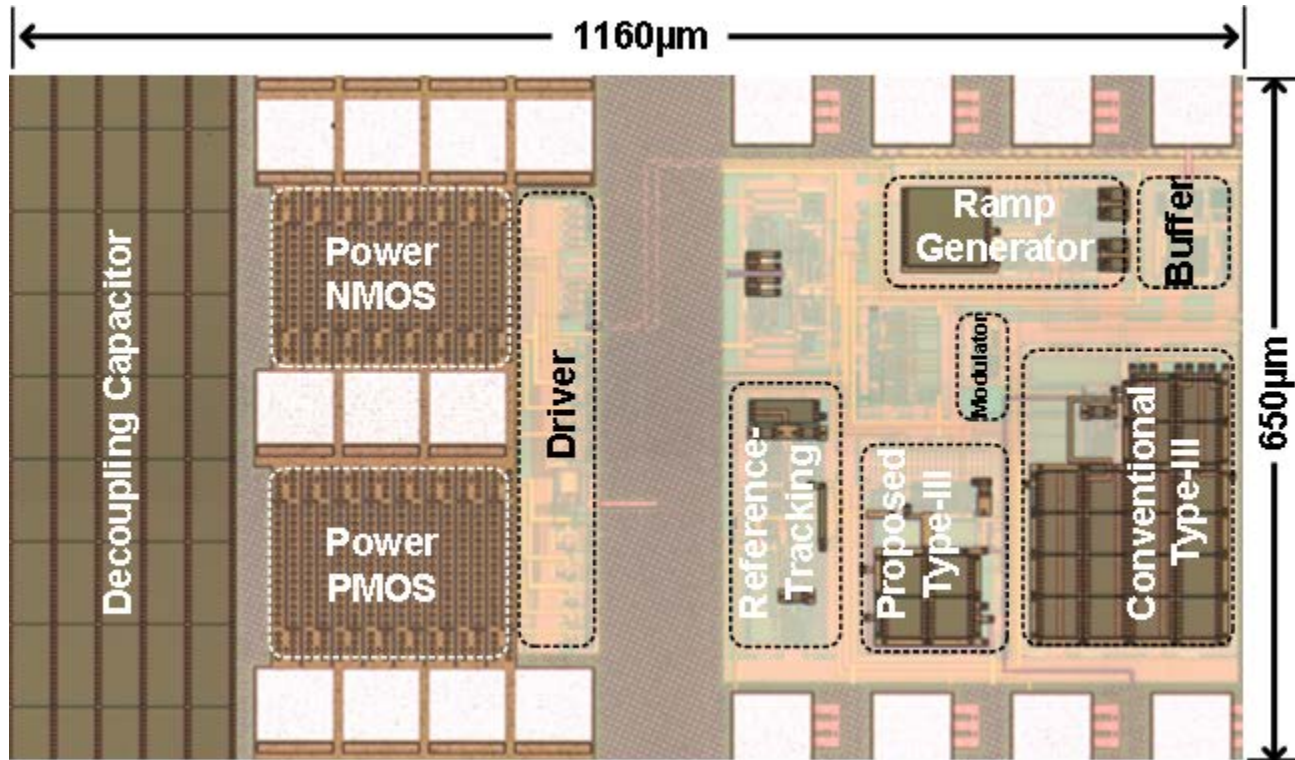
$$\left. \begin{aligned} V_{1+} - V_{1-} &= -(V_{2+} - V_{2-}) \end{aligned} \right\} \Rightarrow \begin{aligned} &V_{2+} = V_{2-} \\ &(V_{Gm} = V_{ref} = V_{fb}) \end{aligned}$$



Outline

- Background
- High-Accuracy Delay-Compensated Ramp Generator
- DDA-Based Type-III Compensator
 - ✓ Area-efficient with simple implementation
 - ✓ Fast reference-tracking scheme
- **Measurement Results**
- Conclusions

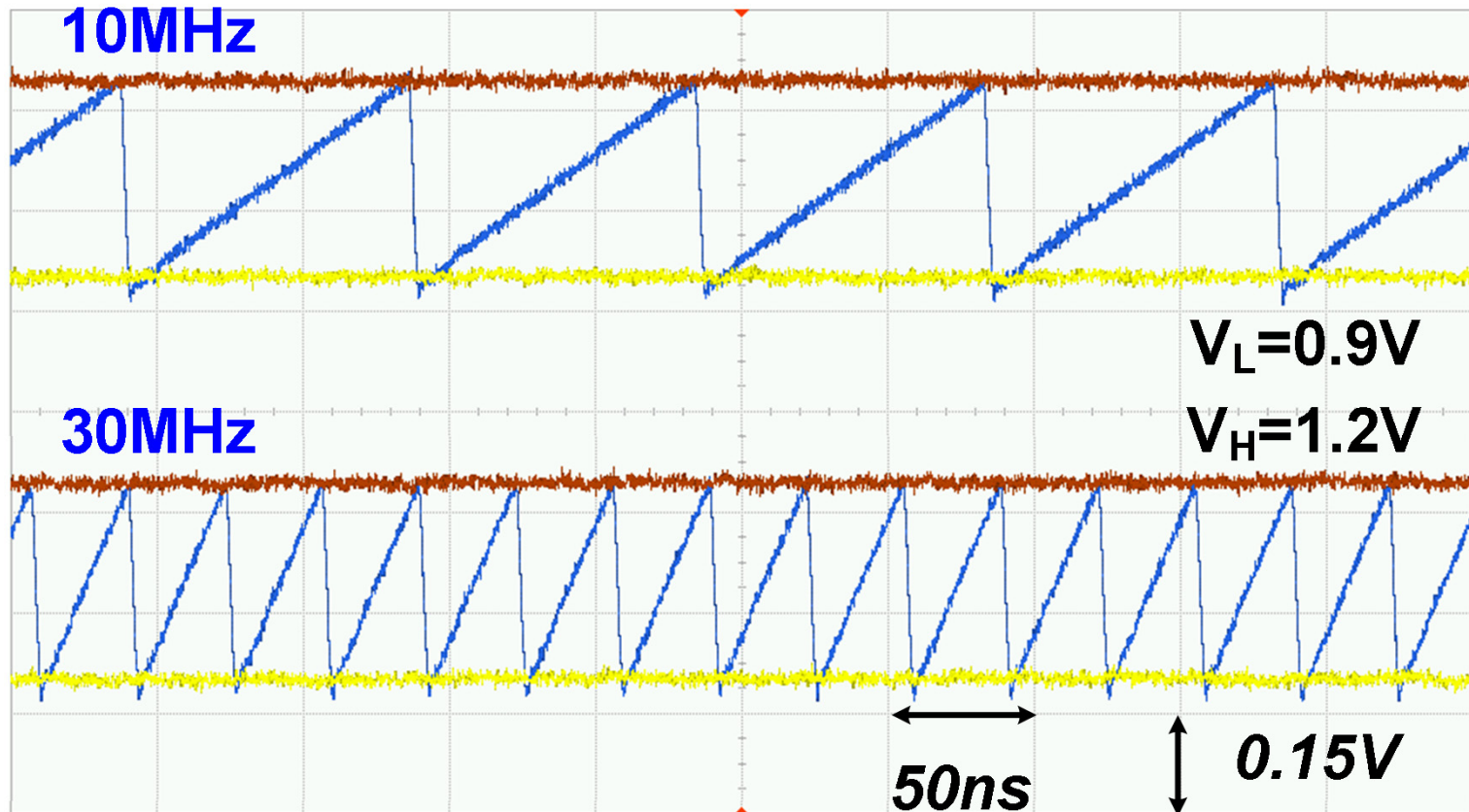
Chip Photo



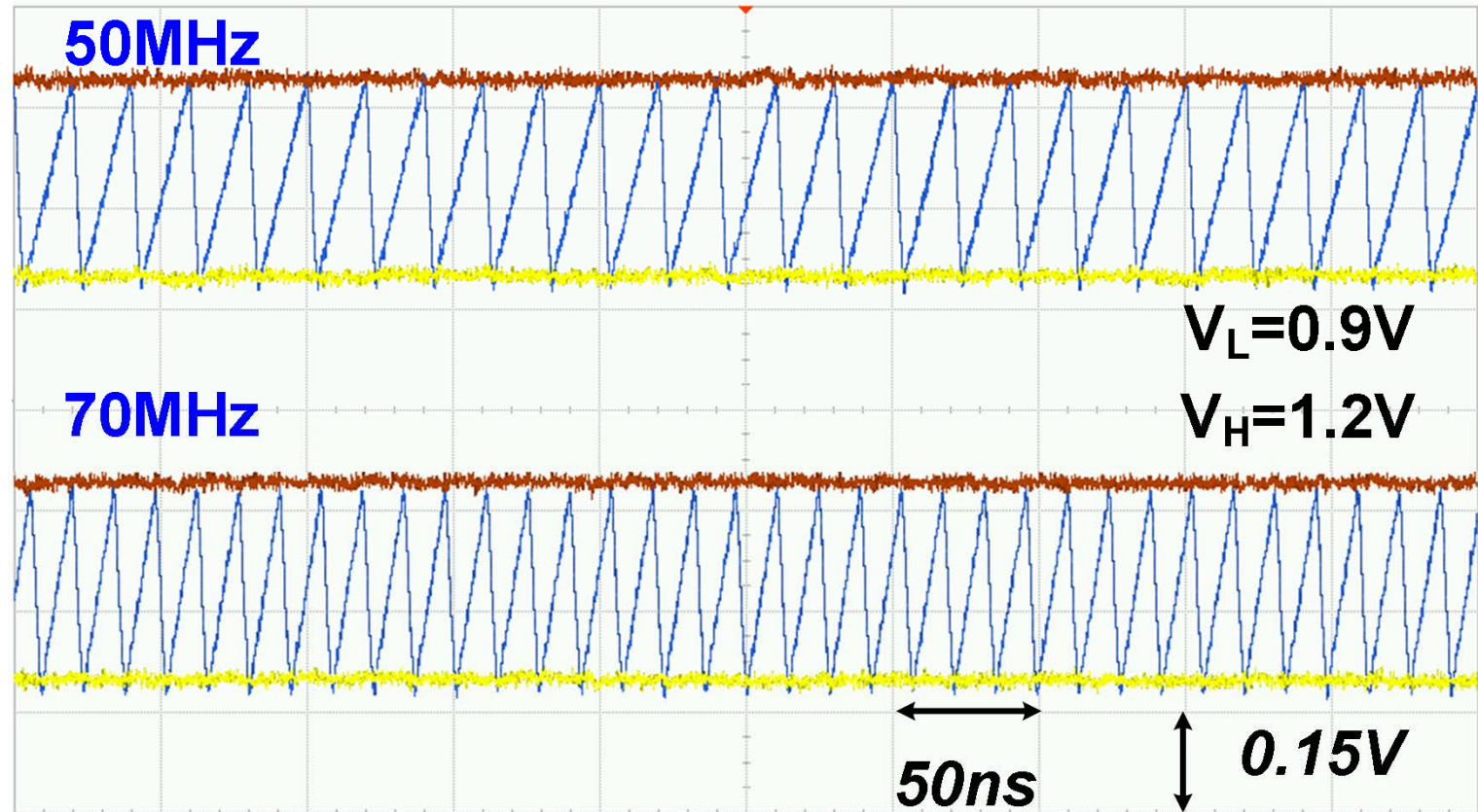
**0.13 μm process
3.3V device**

$$\begin{aligned} f_s &= 10\text{MHz}: L = 0.33\mu\text{H}; C_{\text{out}} = 3.3\mu\text{F} \\ f_s &= 30\text{MHz}: L = 0.33\mu\text{H}; C_{\text{out}} = 1\mu\text{F} \end{aligned}$$

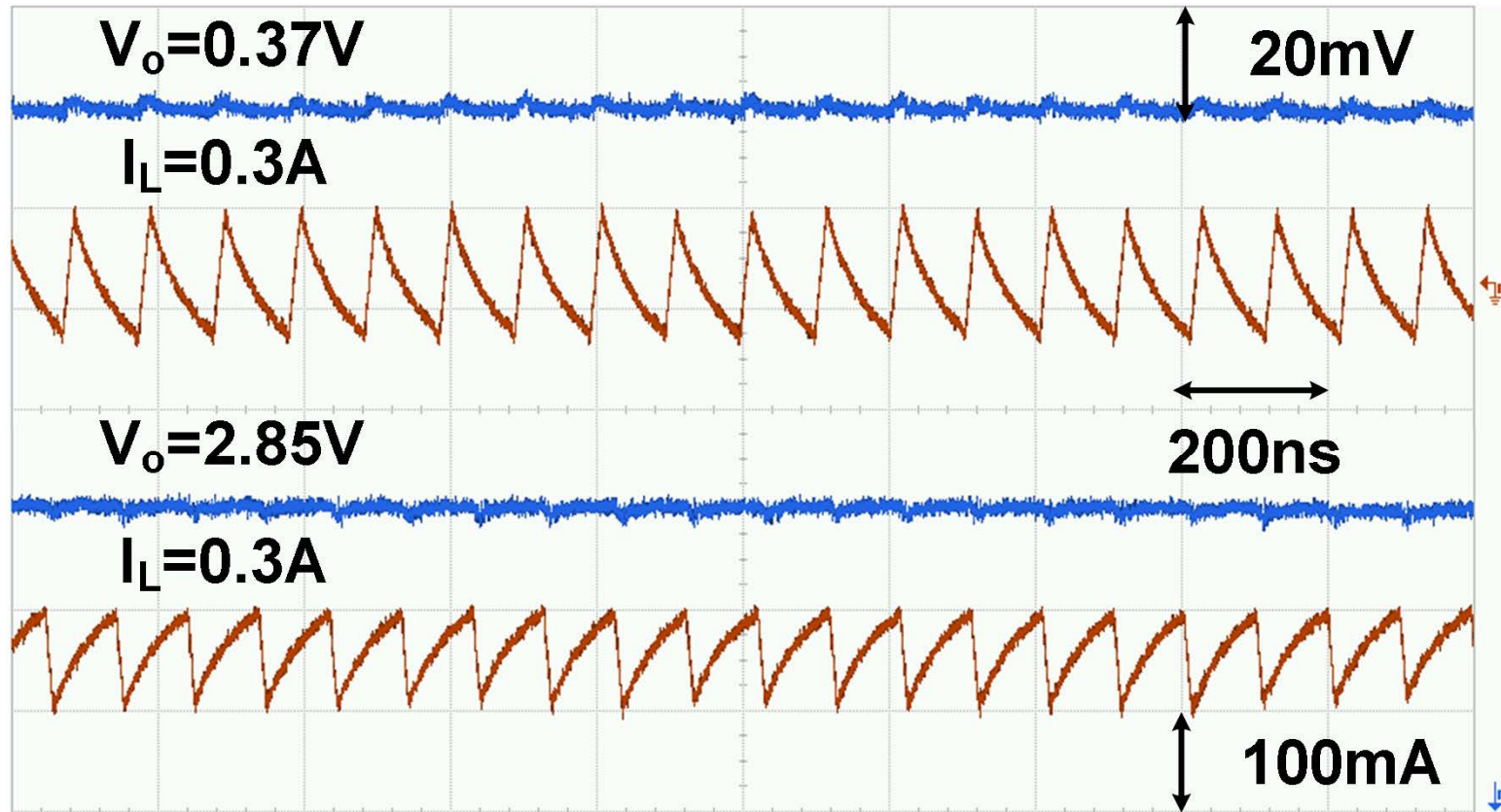
Measurement Results: Ramp Generator



Measurement Results: Ramp Generator



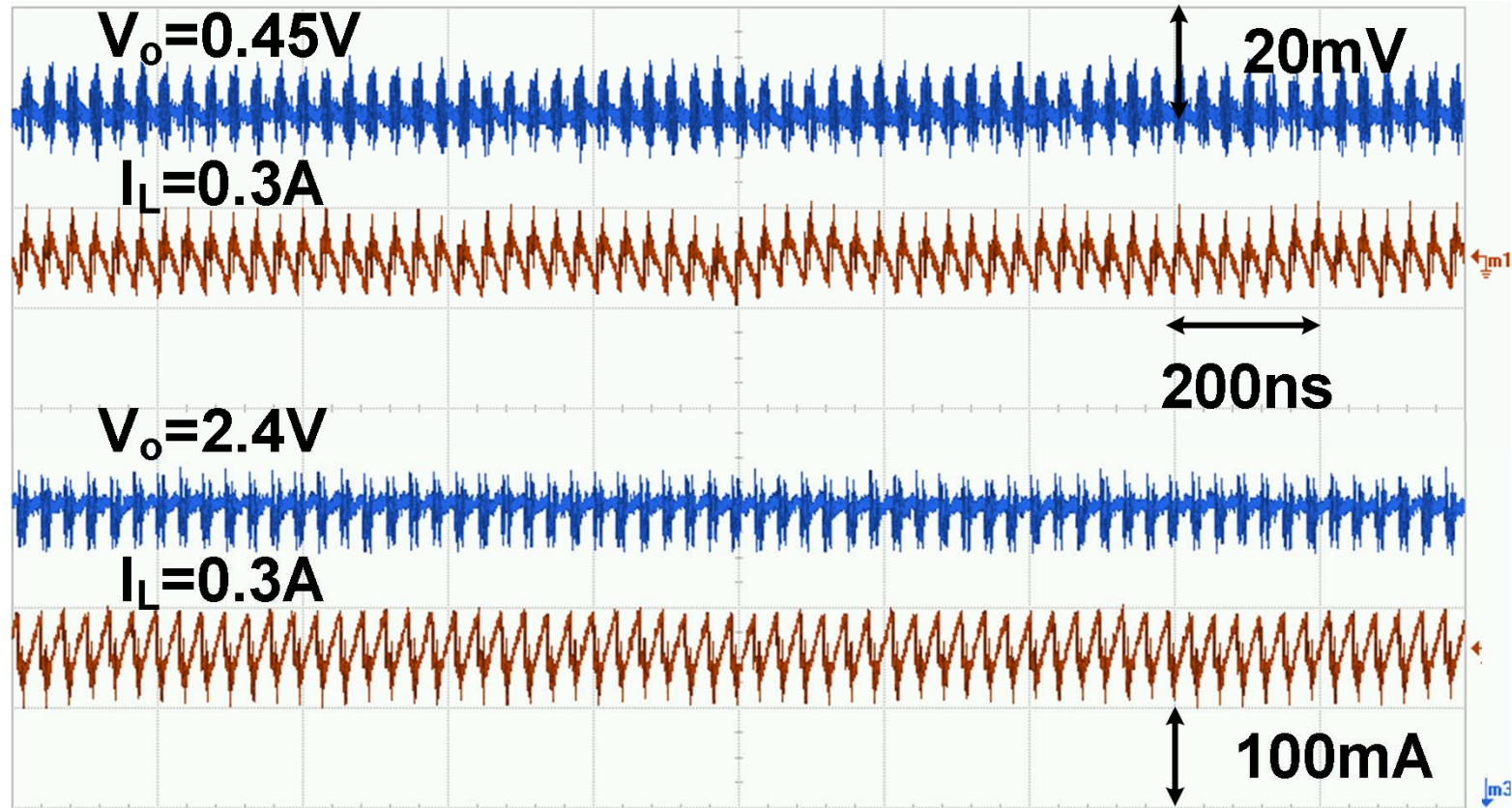
Measurement Results: Steady State



$f_s = 10\text{MHz}; V_g = 3.3\text{V}$

Duty-Cycle Range: $0.86 - 0.11 = 0.75$

Measurement Results: Steady State



$f_s=30\text{MHz}; V_g=3.3\text{V}$

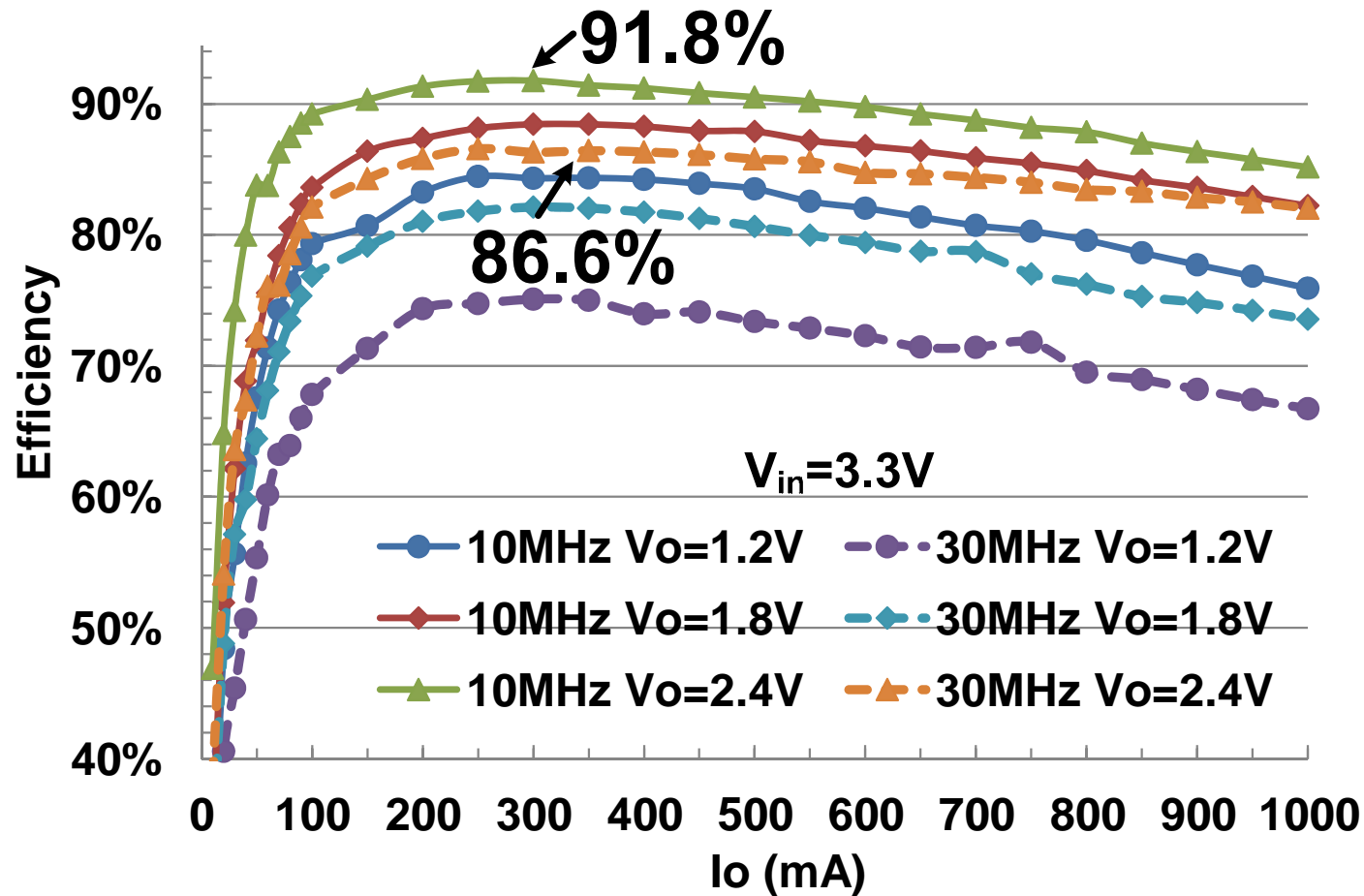
Duty-cycle Range: $0.73-0.14=0.59$

Measurement Results: Steady State

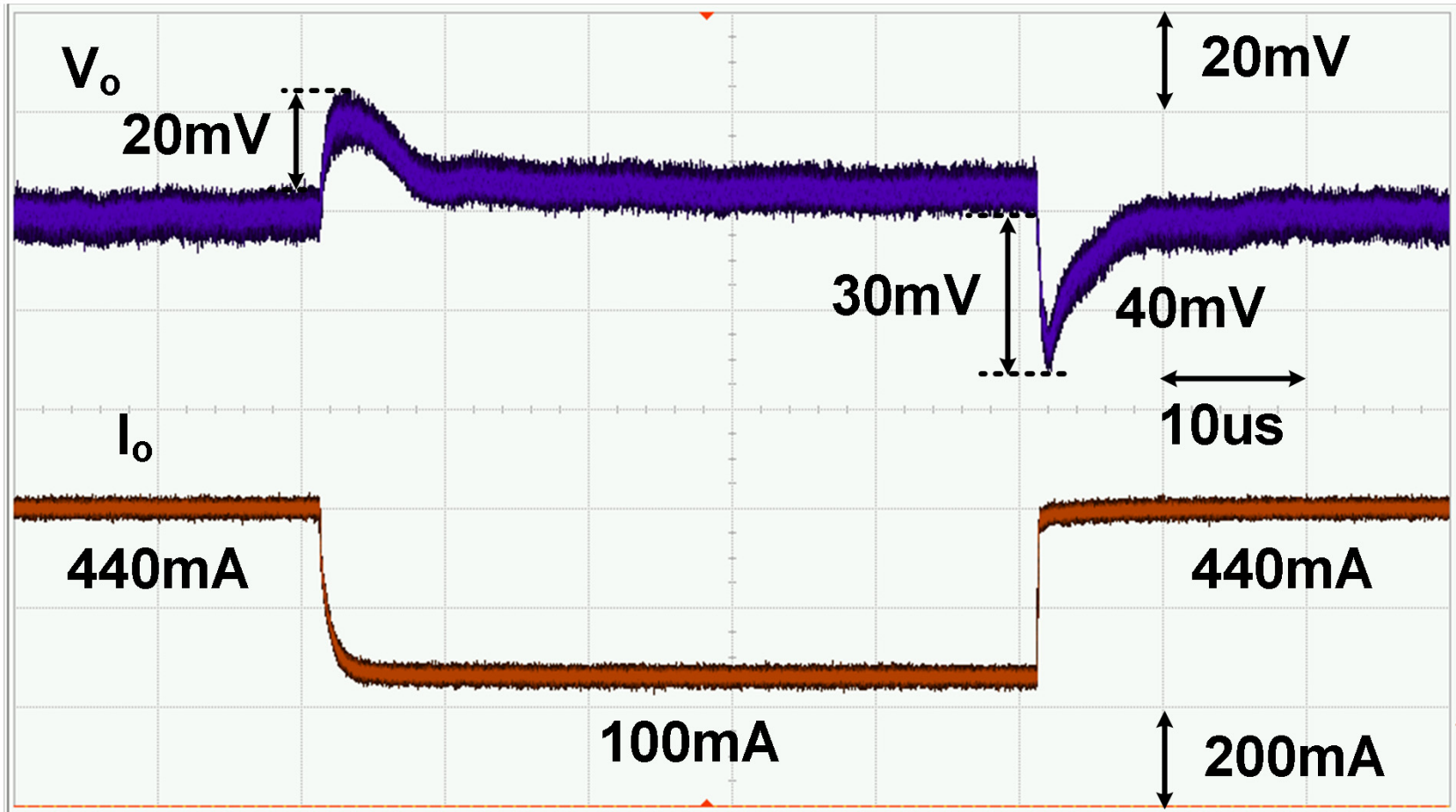
□ Comparison

	[JSSC 2011]		This work	
Control Scheme	Current-Mode		Voltage-Mode	
Switching frequency	3.5MHz	5MHz	10MHz	30MHz
Duty-cycle range	0.78	0.6	0.75	0.59

Measurement Results: Efficiency

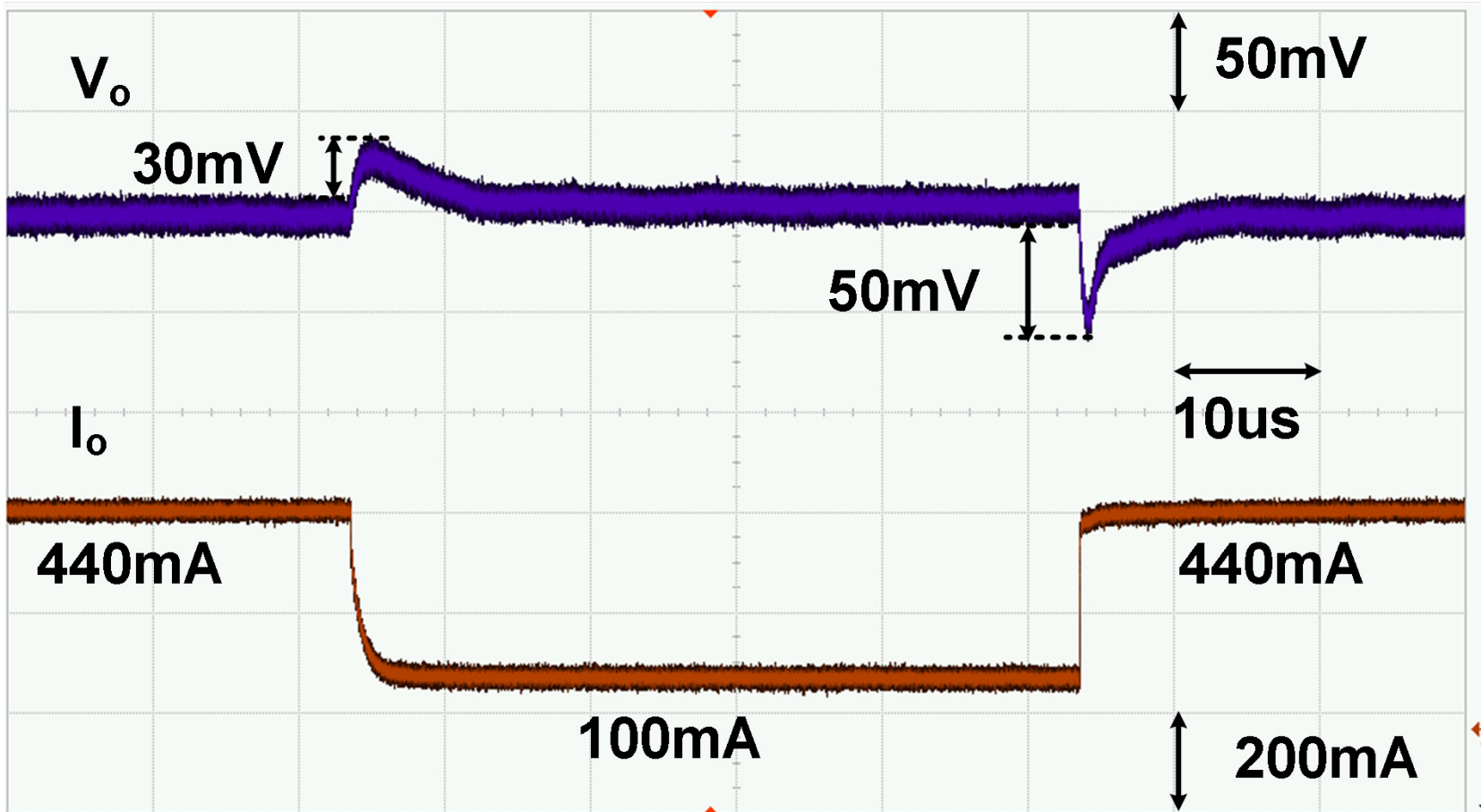


Measurement Results: Load Transient



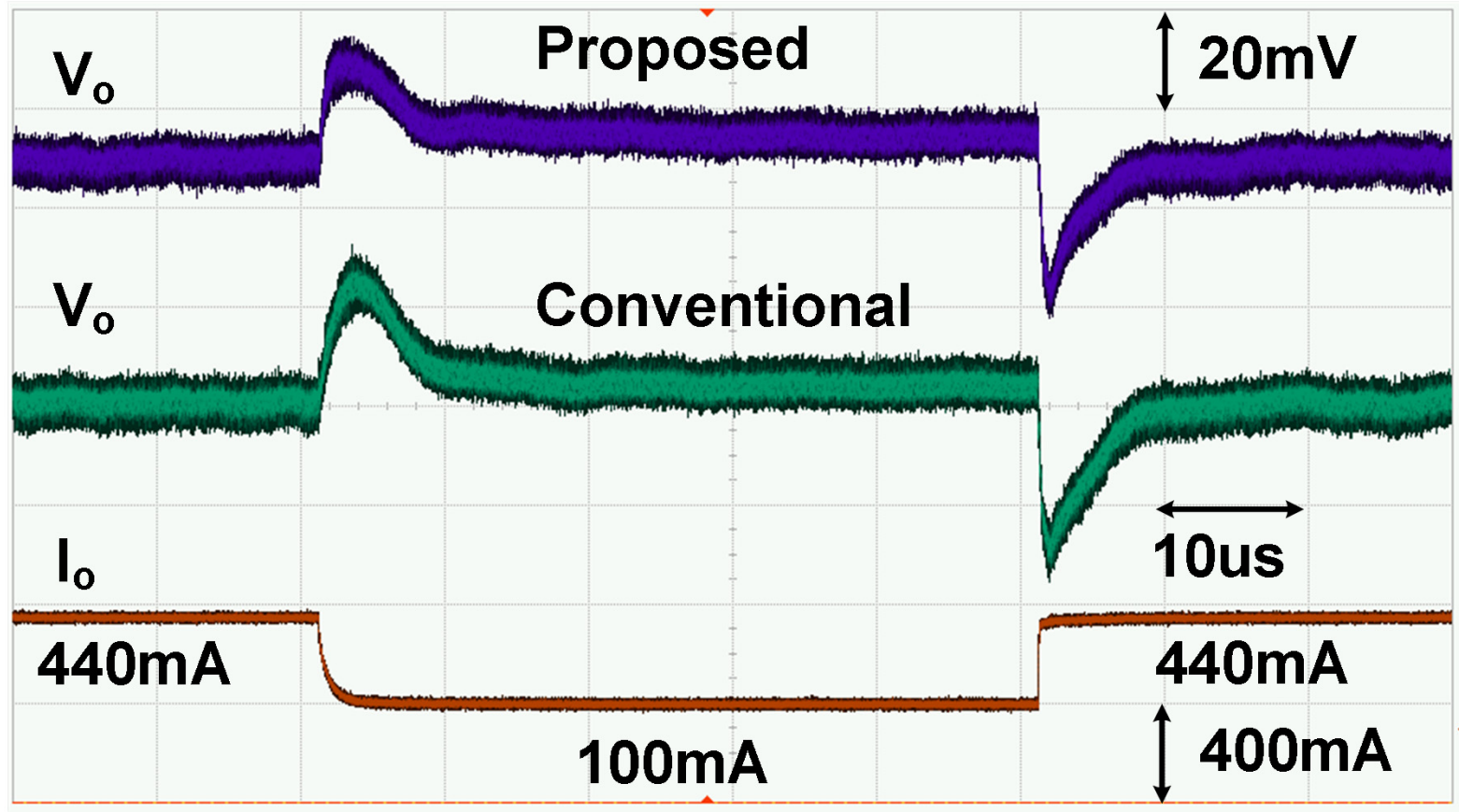
$V_o=1.8V$ $f_s=10MHz$

Measurement Results: Load Transient



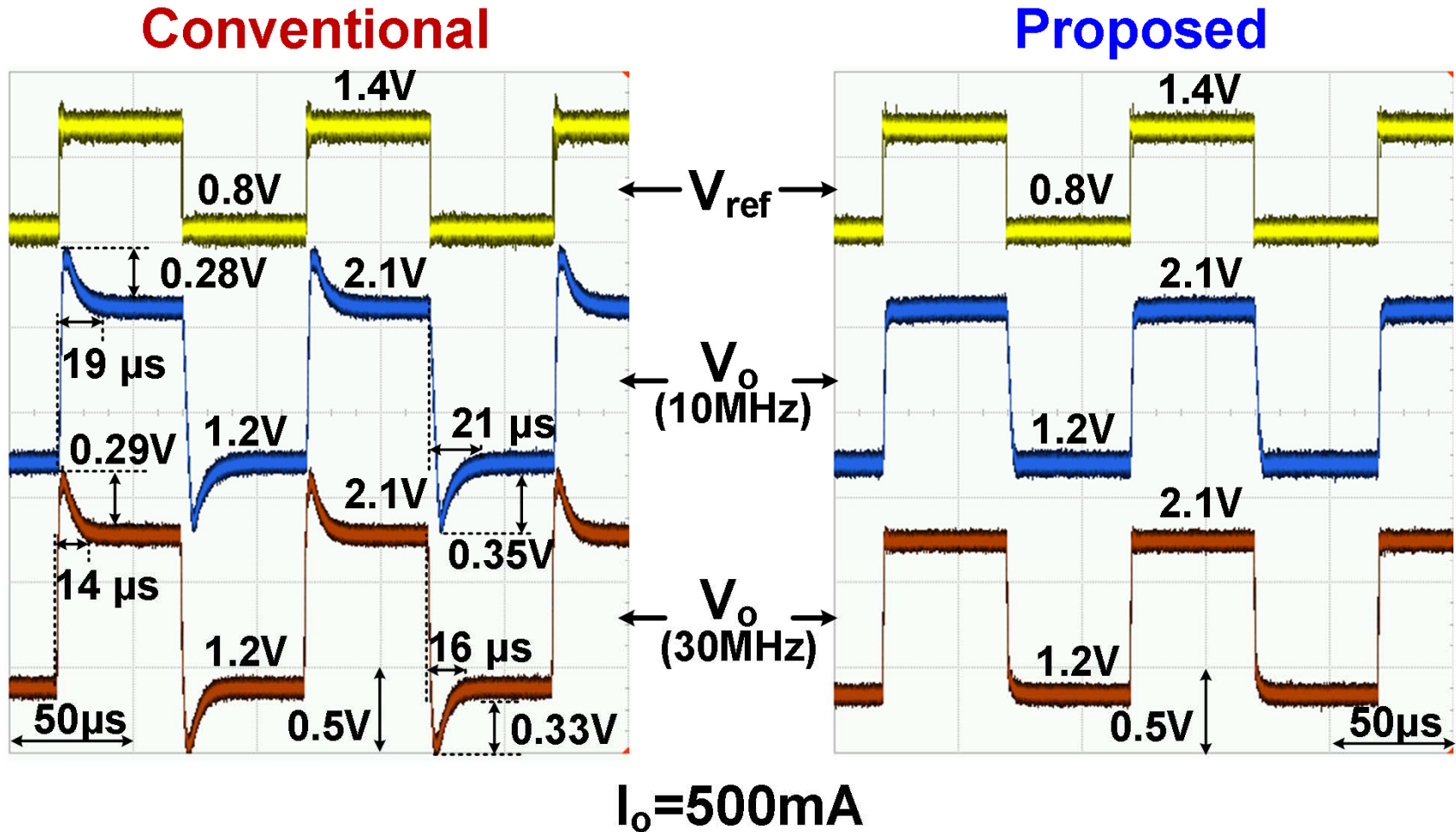
$V_o=1.8V$ $f_s=30MHz$

Measurement Results: Load Transient

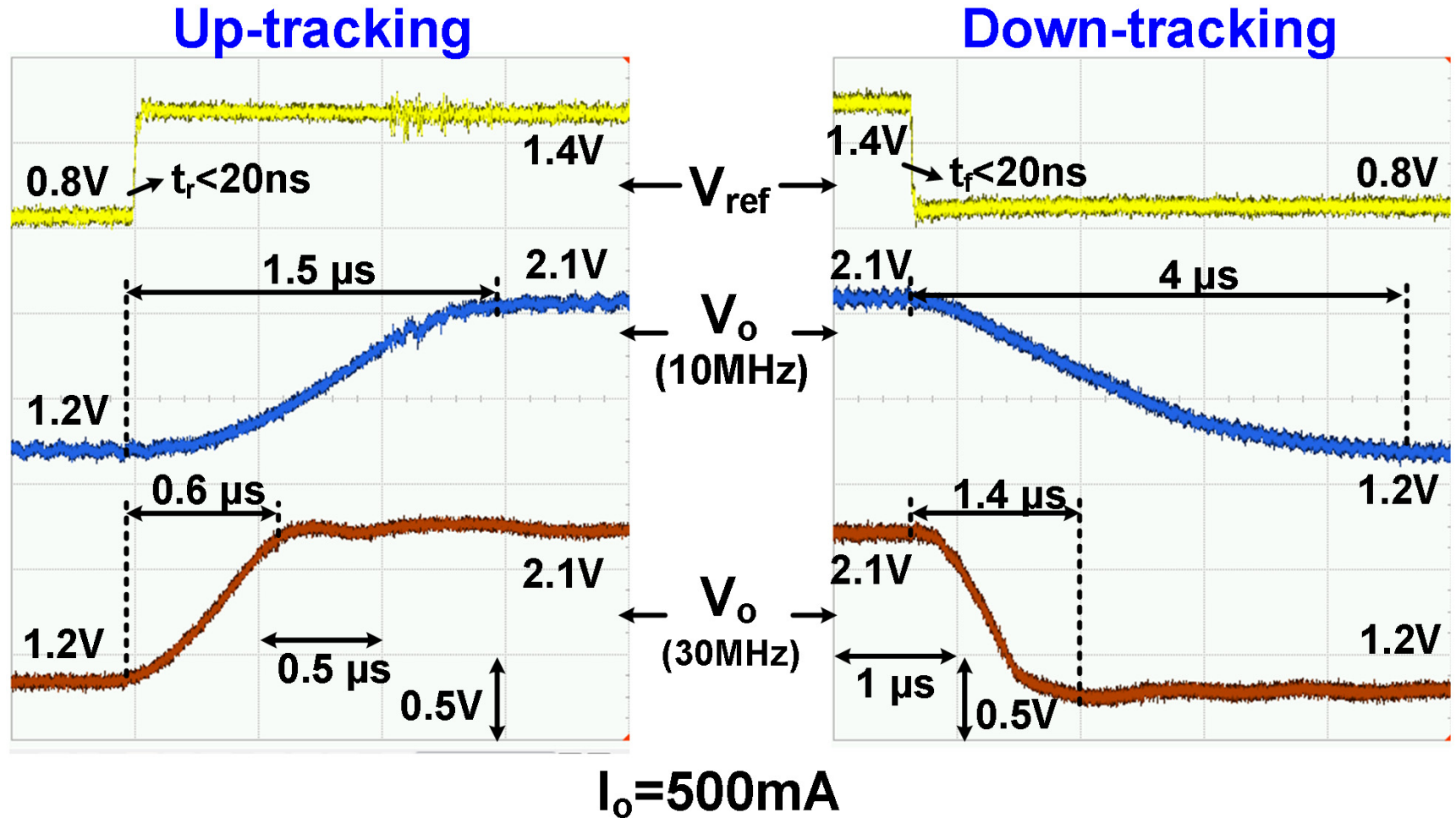


$V_o=1.8V$ $f_s=10MHz$

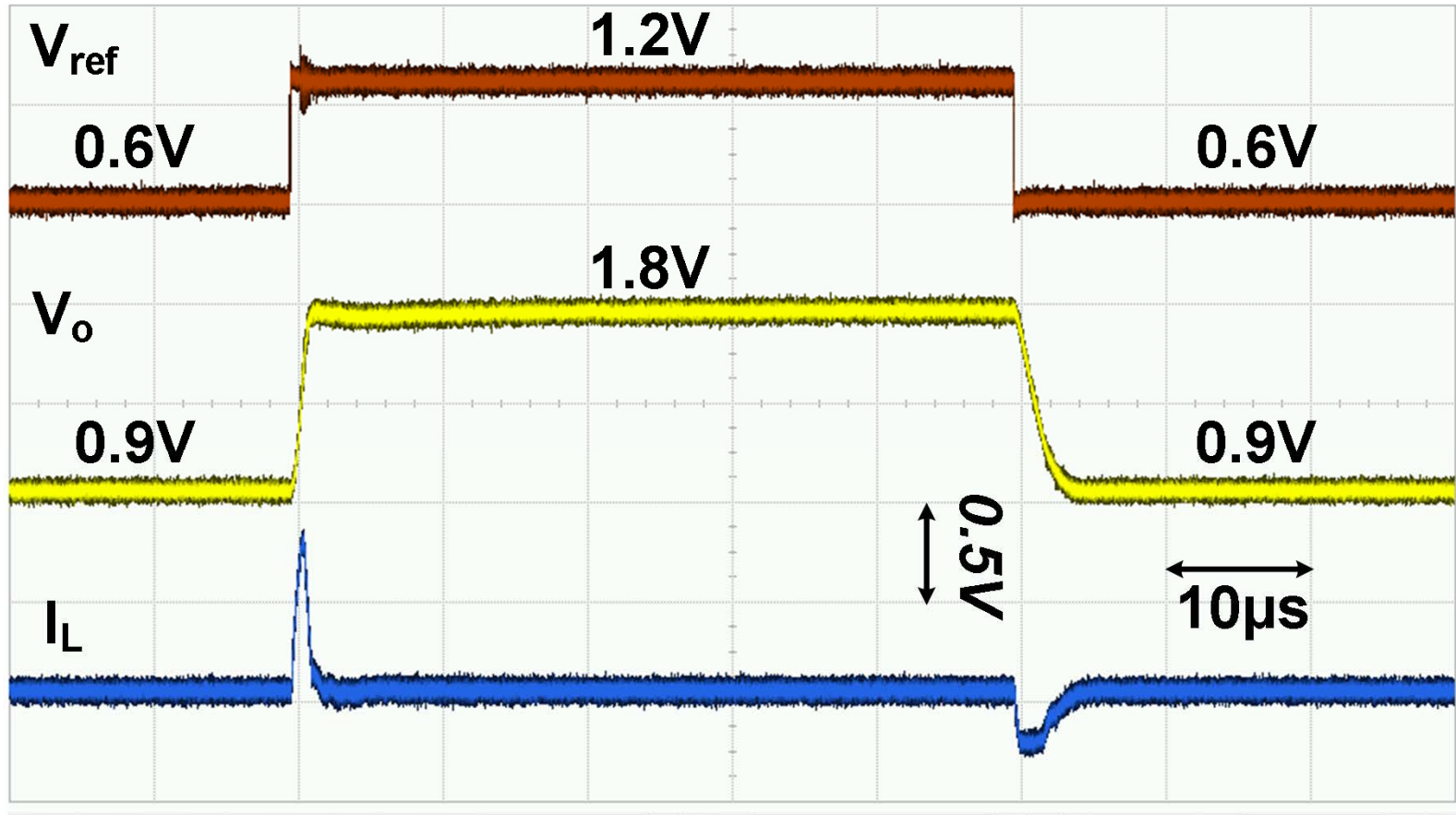
Measurement Results: Reference Tracking



Measurement Results: Reference Tracking

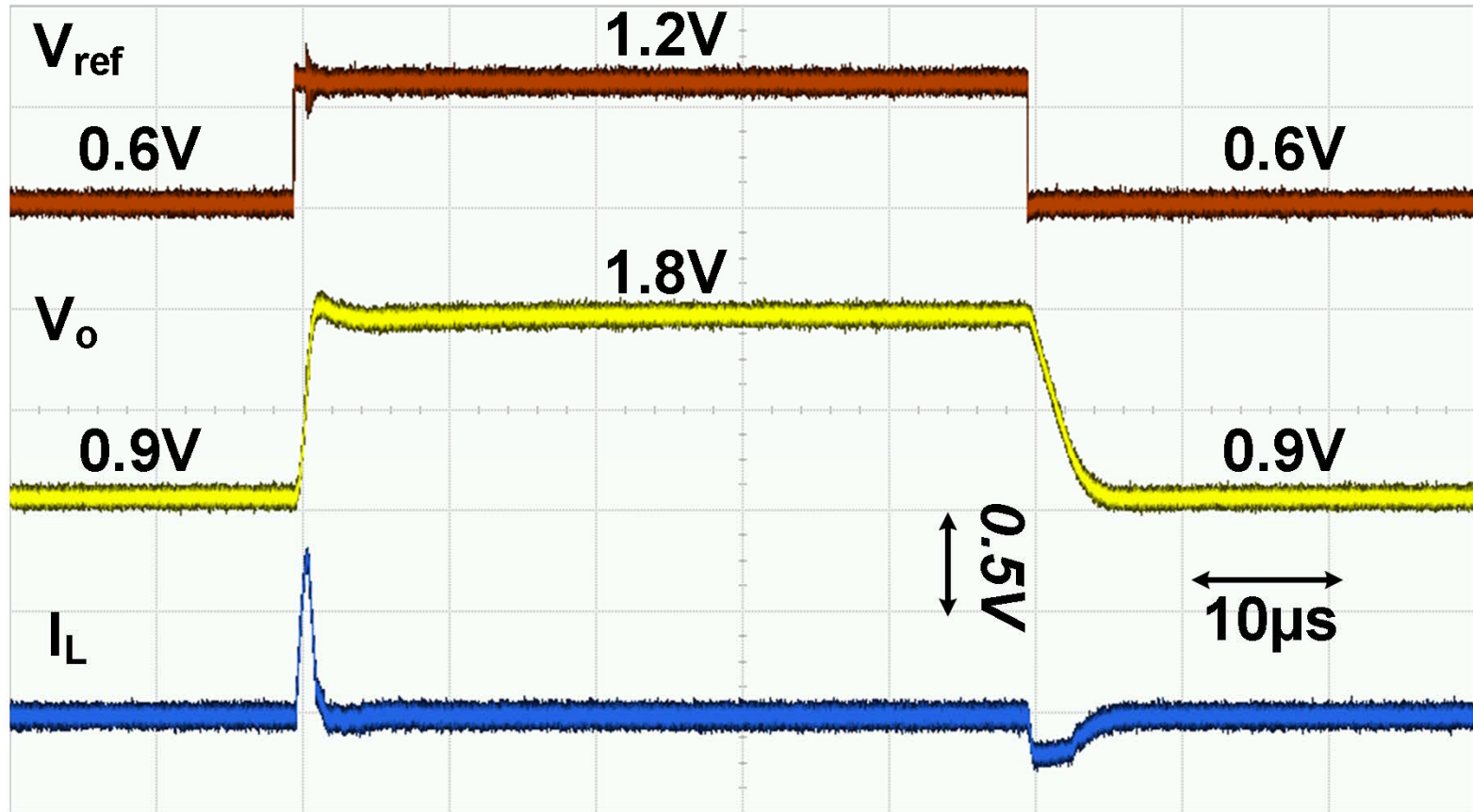


Measurement Results: Reference Tracking



$f_s=10\text{MHz}; I_o=500\text{mA}$

Measurement Results: Reference Tracking



$f_s = 10\text{MHz}$; $I_o = 200\text{mA}$

Comparison

Publication	[JSSC'11]	[JSSC'11]	[TPE'12]	This Work	
Technology	0.13 μ m	0.13 μ m	0.25 μ m	0.13 μ m	
Topology	Buck-Boost	Buck	Buck-Boost	Buck	
Control Scheme	Hysteresis	Voltage-Mode	Current-Mode	Voltage-Mode	
Max. P_{out}	0.4W	0.27W	1.4W	3.6W	
f_{sw}	10MHz	300MHz	5MHz	10MHz	30MHz
L	1 μ H	2nH	1 μ H	0.33 μ H	0.33 μ H
C_{out}	1 μ F	5nF	0.88 μ F	3.3 μ F	1 μ F
Nominal V_g	1.5V	1.2V	2.5~4.5V	3.3V	3.3V
V_{out} Range	0.9~2.2V	0.3~0.88V	3V	0.37~2.85V	0.45~2.4V
Peak Eff.	92.1%	74.5%	91%	91.8%	86.6%
Up-tracking	93.3 μ s/V	2.6 μ s/V	20 μ s/V	1.67 μ s/V	0.67 μ s/V
Down-tracking	26.7 μ s/V	3.6 μ s/V	15 μ s/V	4.44 μ s/V	1.56 μ s/V

Outline

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 - ✓ Fast reference-tracking scheme
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- **Conclusions**

Conclusions

- **High-accuracy delay-compensated ramp generator** is proposed for high frequency DC-DC converters
- **60% area-reduction** and **simple implementation** is achieved by proposed DDA-based Type-III compensator
- **Fastest tracking speed** reported among the state-of-the-art designs by proposed reference-tracking scheme

References

- [1] M. Du, H. Lee, and J. Liu, “A 5-MHz 91% Peak-Power-Efficiency Buck Regulator With Auto-Selectable Peak- and Valley-Current Control,” *IEEE J. Solid-State Circ.*, vol. 46, no.8, pp. 1928 –1939, Aug. 2011.
- [2] P. Y. Wu, S. Y. S. Tsui, and P. K.T. Mok, “Area- and Power-Efficient Monolithic Buck Converters With Pseudo-Type III Compensation,” *IEEE J. Solid-State Circ.*, vol. 45, no. 8, pp. 1446 –1455, Aug. 2010.
- [3] E. Sackinger and W. Guggenbuhl, “A Versatile Building Block: The CMOS Differential Difference Amplifier,” *IEEE J. Solid-State Circ.*, vol. 22, no. 2, pp. 287–294, Apr. 1987.
- [4] C. Zheng and D. Ma, “A 10-MHz Green-Mode Automatic Reconfigurable Switching Converter for DVS-Enabled VLSI Systems,” *IEEE J. Solid-State Circ.*, vol. 46, no. 6, pp. 1464 –1477, Jun. 2011.
- [5] S. S. Kudva and R. Harjani, “Fully-Integrated On-Chip DC-DC Converter With a 450X Output Range,” *IEEE J. Solid-State Circ.*, vol. 46, no. 8, pp. 1940–1951, 2011.
- [6] Y.-H. Lee, et al, “Power-Tracking Embedded Buck-Boost Converter With Fast Dynamic Voltage Scaling for the SoC System,” *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1271–1282, 2012.

Thank you 😊

ISSCC 2014
4.5

A 2-PHASE RESONANT SWITCHED CAPACITOR CONVERTER DELIVERING 4.3 W AT 0.6 W/mm² WITH 85 % EFFICIENCY

Kapil Kesarwani, Rahul Sangwan and Jason T. Stauth

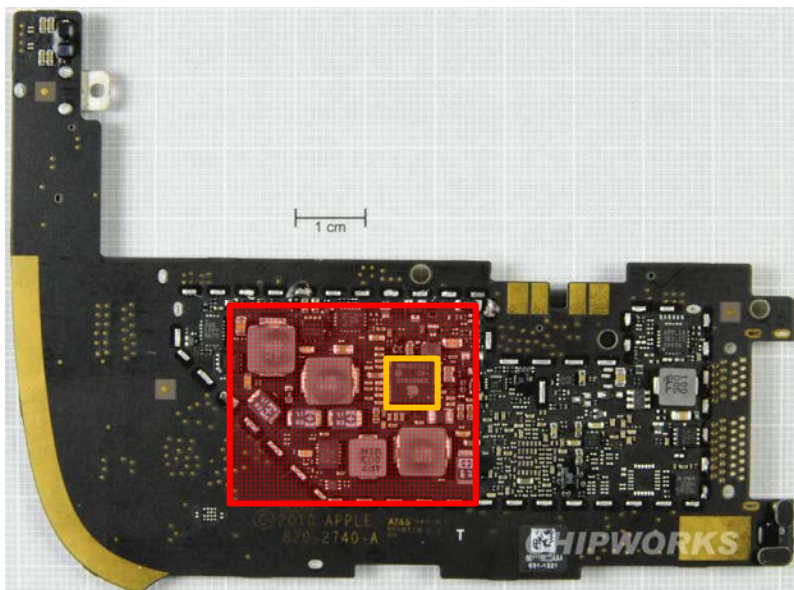
**Thayer School of Engineering
at Dartmouth**



THAYER SCHOOL OF
ENGINEERING
AT DARTMOUTH



Power converters in portable electronics



iPad 1st Generation



PMIC



PMIC + passive elements

Pictures from
www.chipworks.com

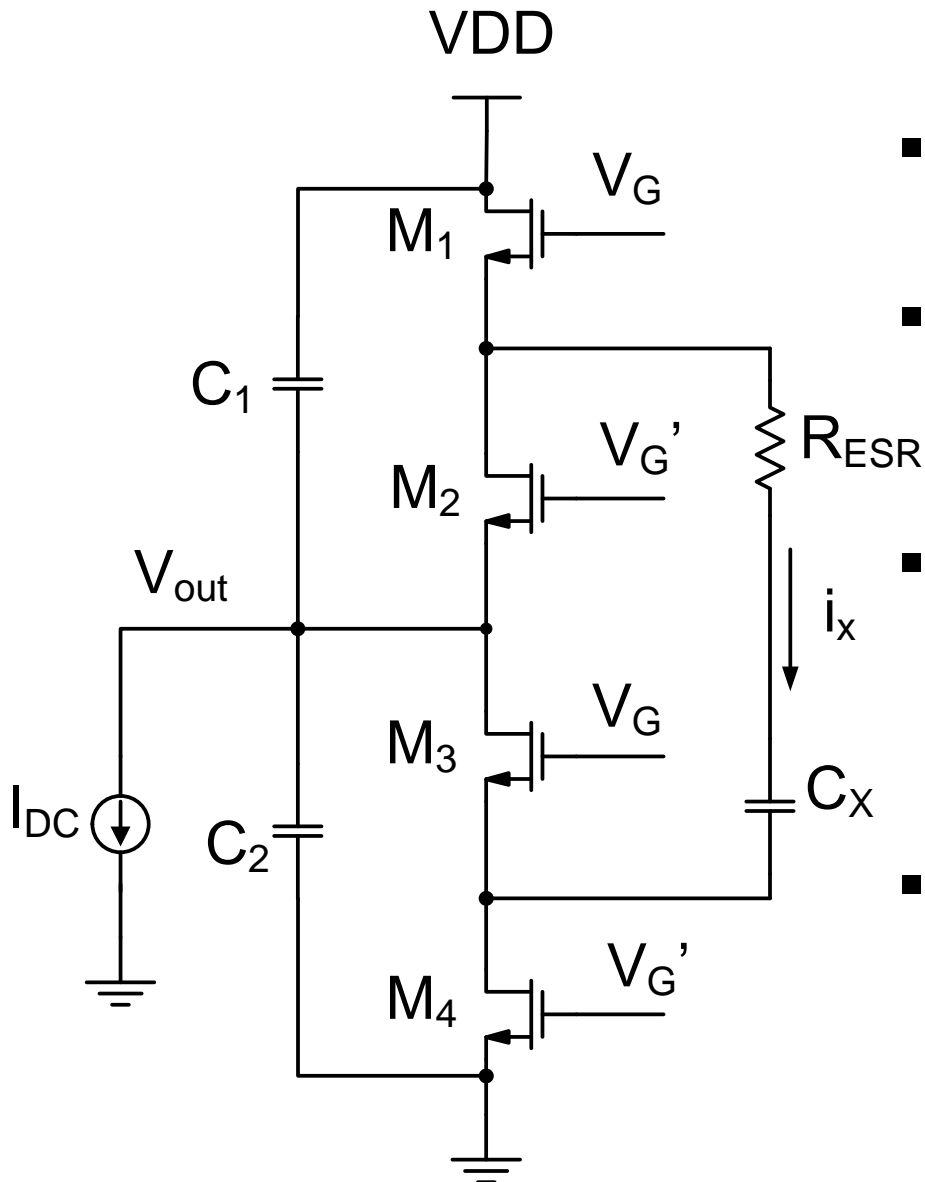
- Digital system complexity
 - Increasing Parallelism (multiple cores)
 - Constrained Power Density
- Multiple off-chip supplies increase motherboard complexity
- Power converters occupy 20%-30% of the total volume in modern electronic devices

→ Increasing need for fully integrated power management

Overview

- First Chip-Scale Resonant Switched Capacitor (ReSC) converter
 - Discussion
 - Modeling
 - Design and Implementation
- Dynamic Off-Time Modulation (DOTM)
 - Adds load-line regulation capability to the ReSC converter
 - Maintains peak efficiency in light-load

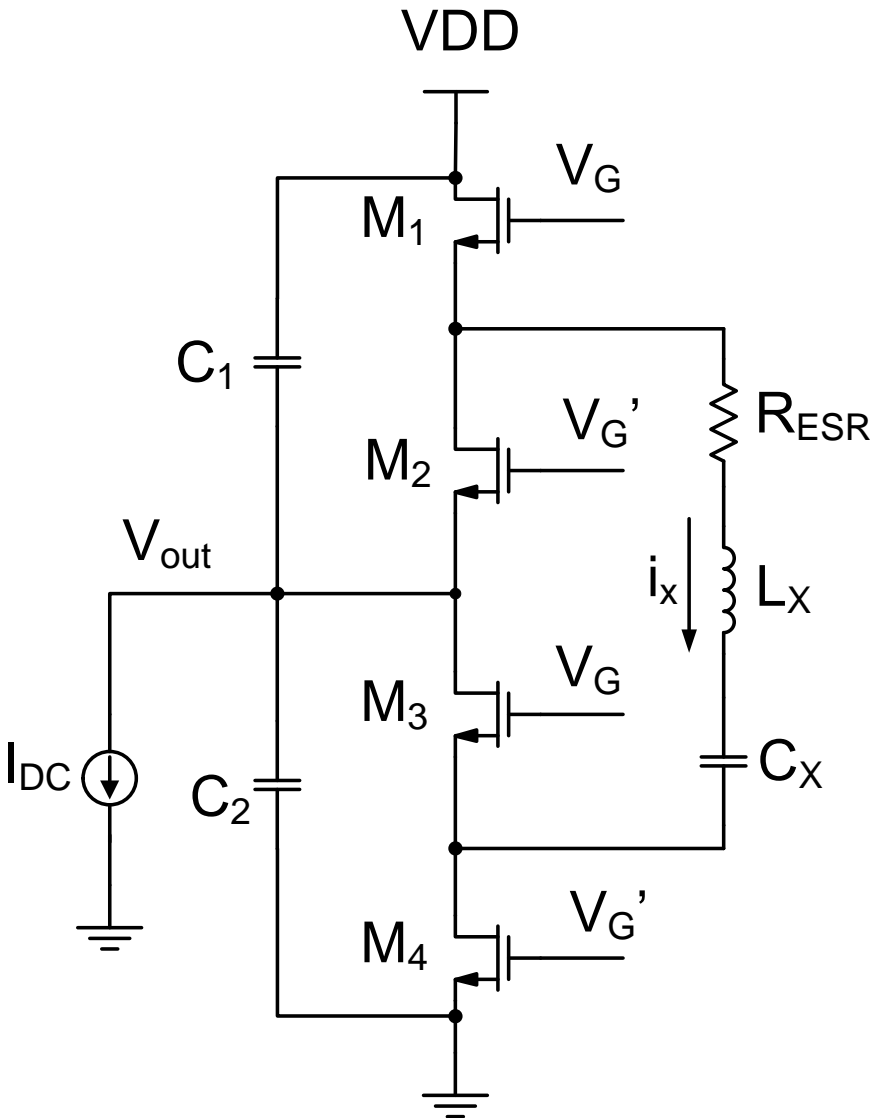
Switched Capacitor Converters



- Prime candidate for integrated DC-DC converters
- Eliminate inductors and utilize high-density integrated capacitors
- Achieve **higher device utilization FOM*** compared to traditional DC-DC converter topologies
- Emergence of high-density deep-trench capacitors

*M. D. Seeman et. al, *IEEE TPEL*, 2008

Resonant Switched Capacitor Converters



Similarities to SC Converters:

- Similar architectures (Dickson, Series-Parallel, etc)
- Maintain favorable device utilization FOMs
- Leverage high-density capacitors

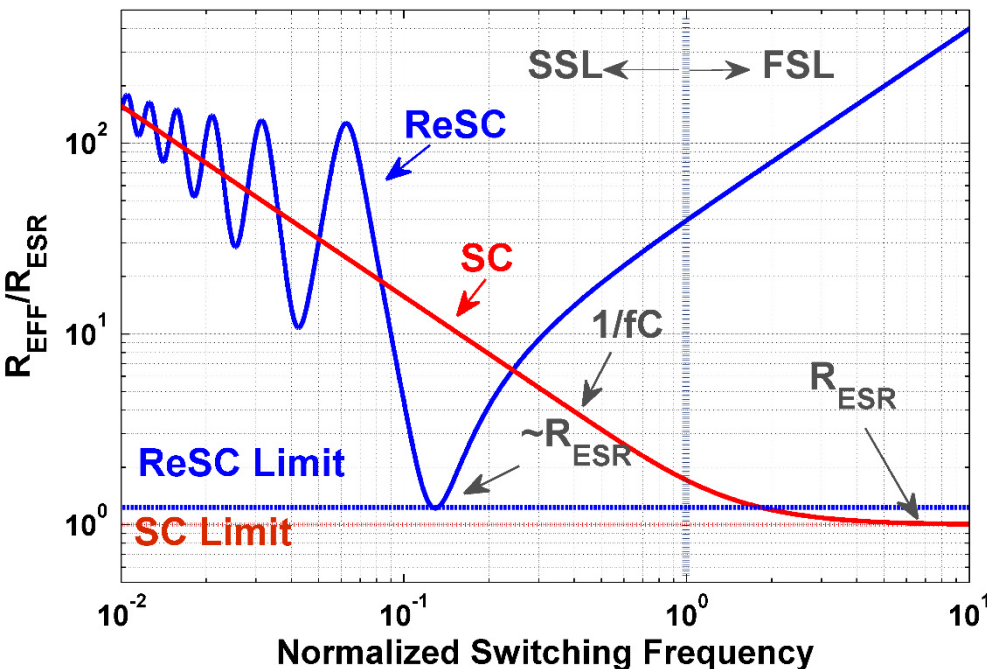
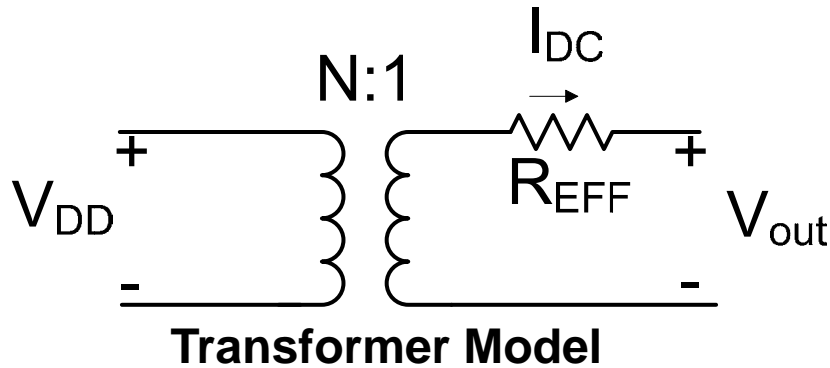
Advantages of ReSC:

- Small magnetic component (few nH) resonates out reactive impedance
- Improved trade-offs between switching and conduction loss
- Narrowband energy transfer
- Zero current switching

J. T. Stauth et. al. , ISSCC, 2012

4.5: A 2-PHASE RESONANT SWITCHED CAPACITOR CONVERTER DELIVERING 4.3 W
AT 0.6 W/mm² WITH 85 % EFFICIENCY

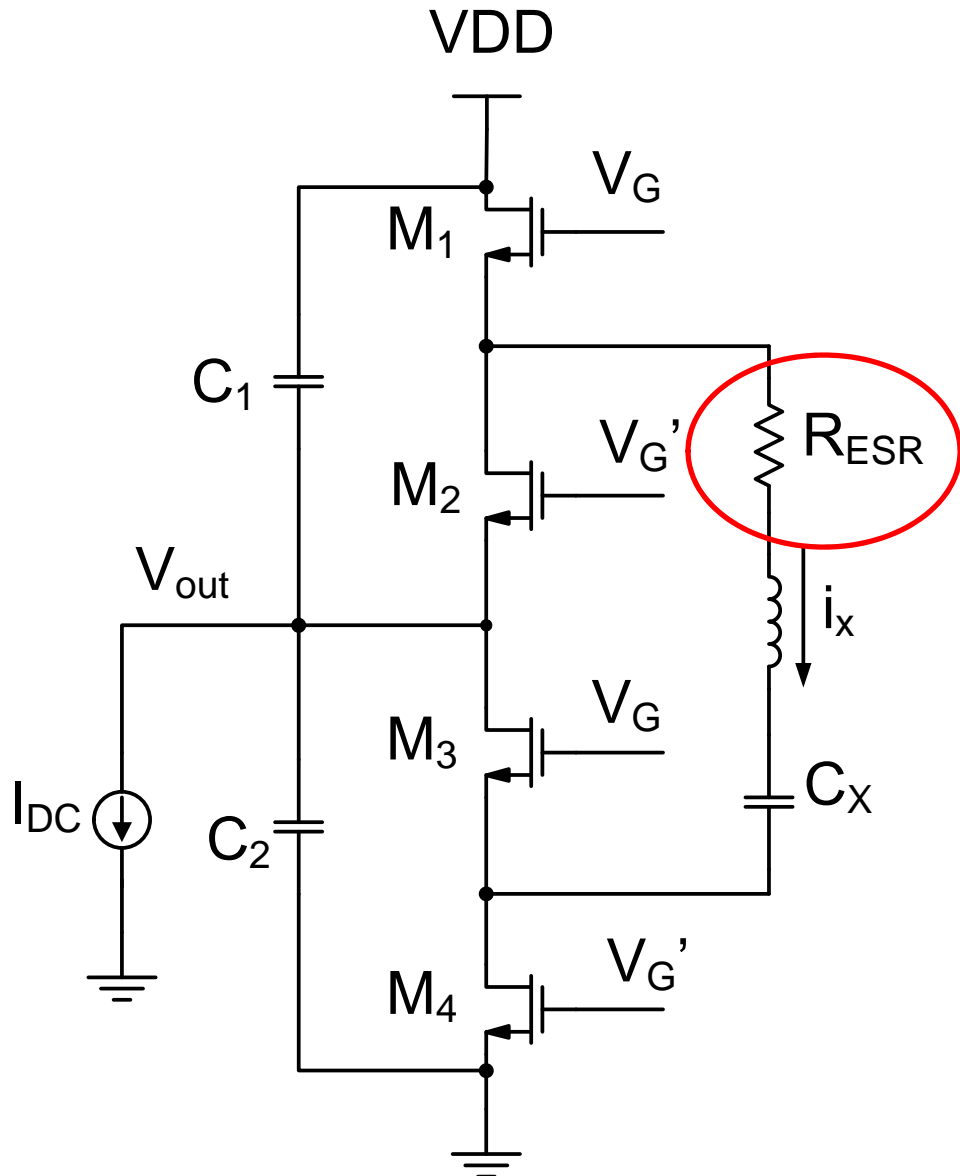
Effective Resistance



- R_{EFF} models the effective output impedance of the converter
- SC: In fast switching mode the energy transfer is limited by ESR
- ReSC converter achieve similar effective resistance as SC converter but at a lower frequency
- Opportunities for fundamental or sub-harmonic operation

Modeling for Chip-Scale Implementation

Modeling: ReSC Converter



- R_{ESR} includes:
 - AC Resistance of Inductor
 - Capacitor ESR
 - Interconnect Resistance
 - Switch 'on' Resistance
- Bottom plate capacitance is also considered
- Bypass capacitance
 - Required for voltage ripple
 - Part of resonant loop

Loss Optimization

$$R_{ESR} = \frac{2R_{on,sp}}{W_{sw}} + R_{Lx}(f) + R_{Cx}(f)$$

Switch
Resistance

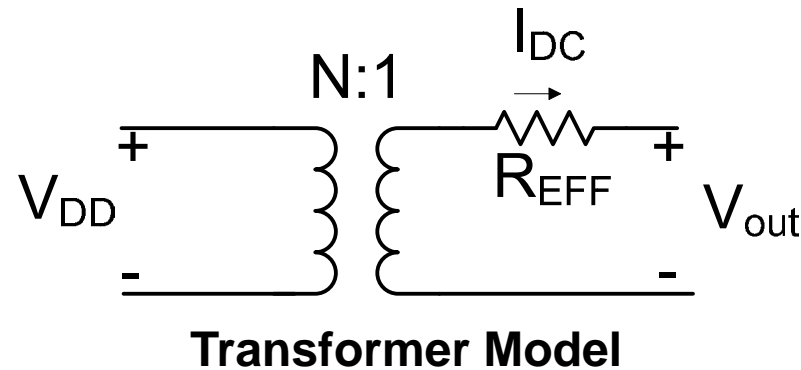
Inductor ESR

Capacitor ESR

Conduction Loss $\rightarrow P_{cond} = I_{DC}^2 R_{EFF}$

$$R_{EFF} \approx \frac{1}{4f_{sw}C_X} \tanh\left(\frac{R_{ESR}}{8f_{sw}L_X}\right)$$

$\rightarrow f_{sw}$ is the resonant switching frequency



Transformer Model

Loss Optimization

Switching Loss $\rightarrow P_{sw} = 4C_{in,sp} W_{SW} V_G^2 f_{sw} + C_{BOT} V_{OUT}^2 f_{sw}$

Input Gate Capacitance Loss

Bottom Plate loss

Total Loss $\rightarrow P_{loss} = \underbrace{4C_{in,sp} W_{SW} V_G^2 f_{sw} + C_{BOT} V_{OUT}^2 f_{sw}}_{\text{Switching Loss}} + \underbrace{I_{DC}^2 R_{EFF}}_{\text{Conduction Loss}}$

Optimization Variables:

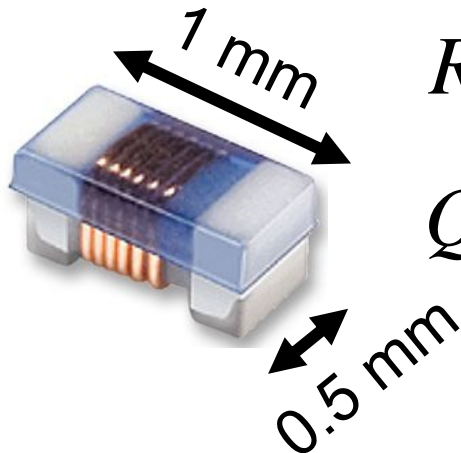
- Switch Width (W_{SW})
- Switching Inductor (L_X)
- Switching Capacitor (C_X)

$$f_{SW} = f(W_{SW}, L_X, C_X)$$

Design Procedure

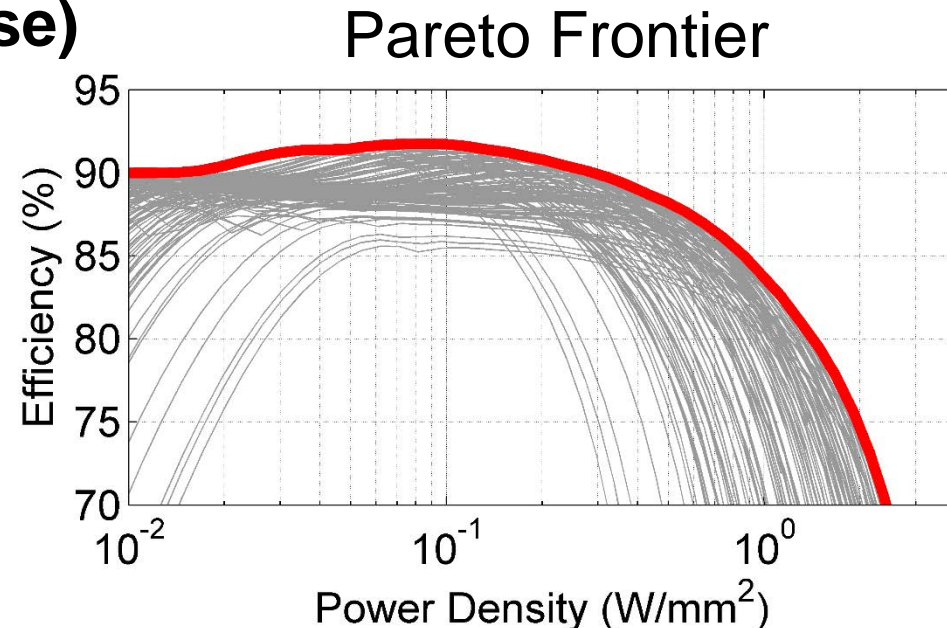
- Multivariable Pareto Optimization
 - Loss Model (switch sizing, component Q)
 - Switching Frequency (resonant Frequency)
 - Component Selection (Cap sizing and inductor model)

**Die-Attach Air-Core Solenoid
(SMT small-footprint Database)
'mm² – scale' components**



$$R_{AC} \propto \sqrt{f_{SW}}$$

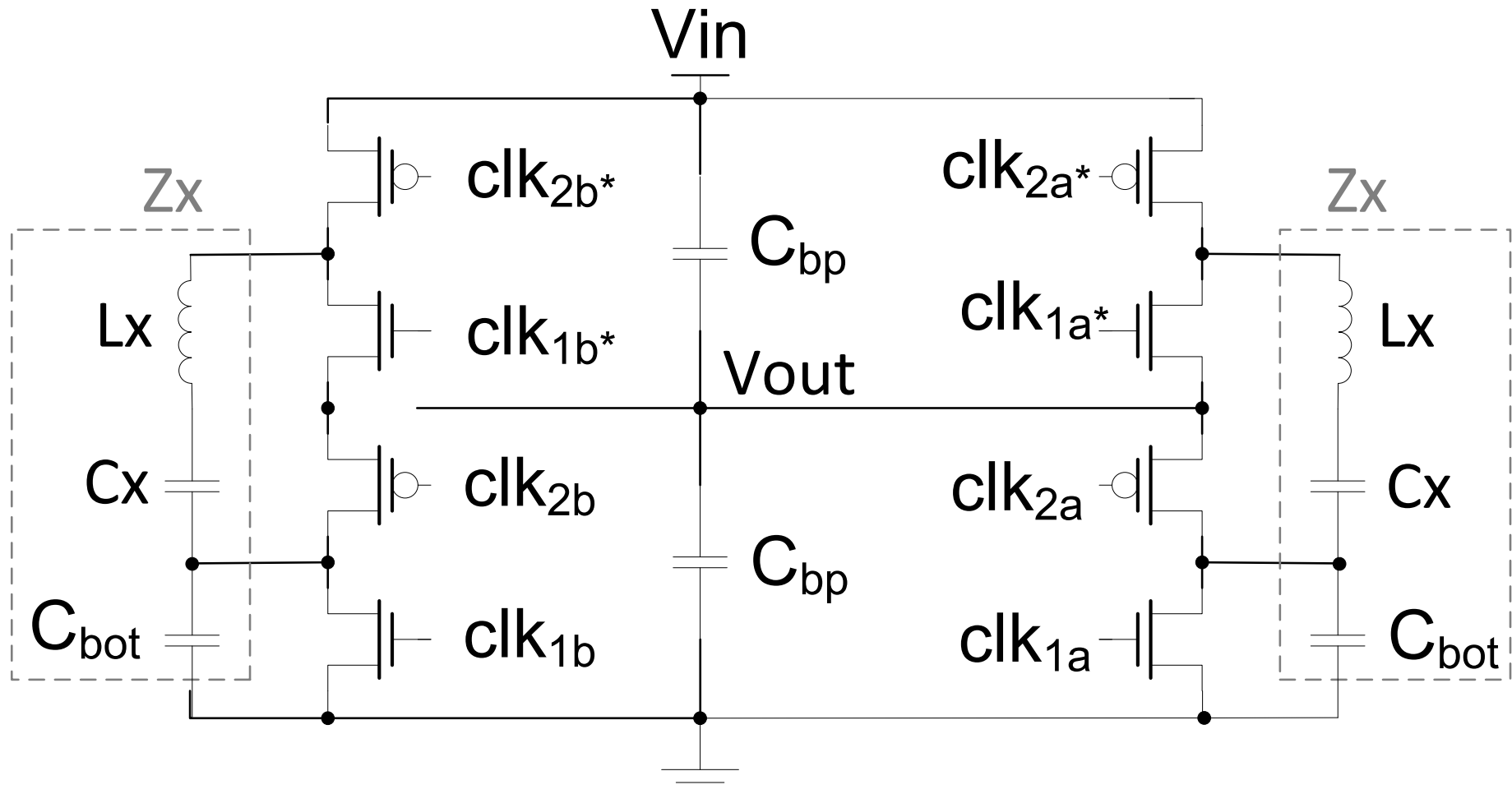
$$Q \propto \sqrt{f_{SW}}$$



Design Parameters

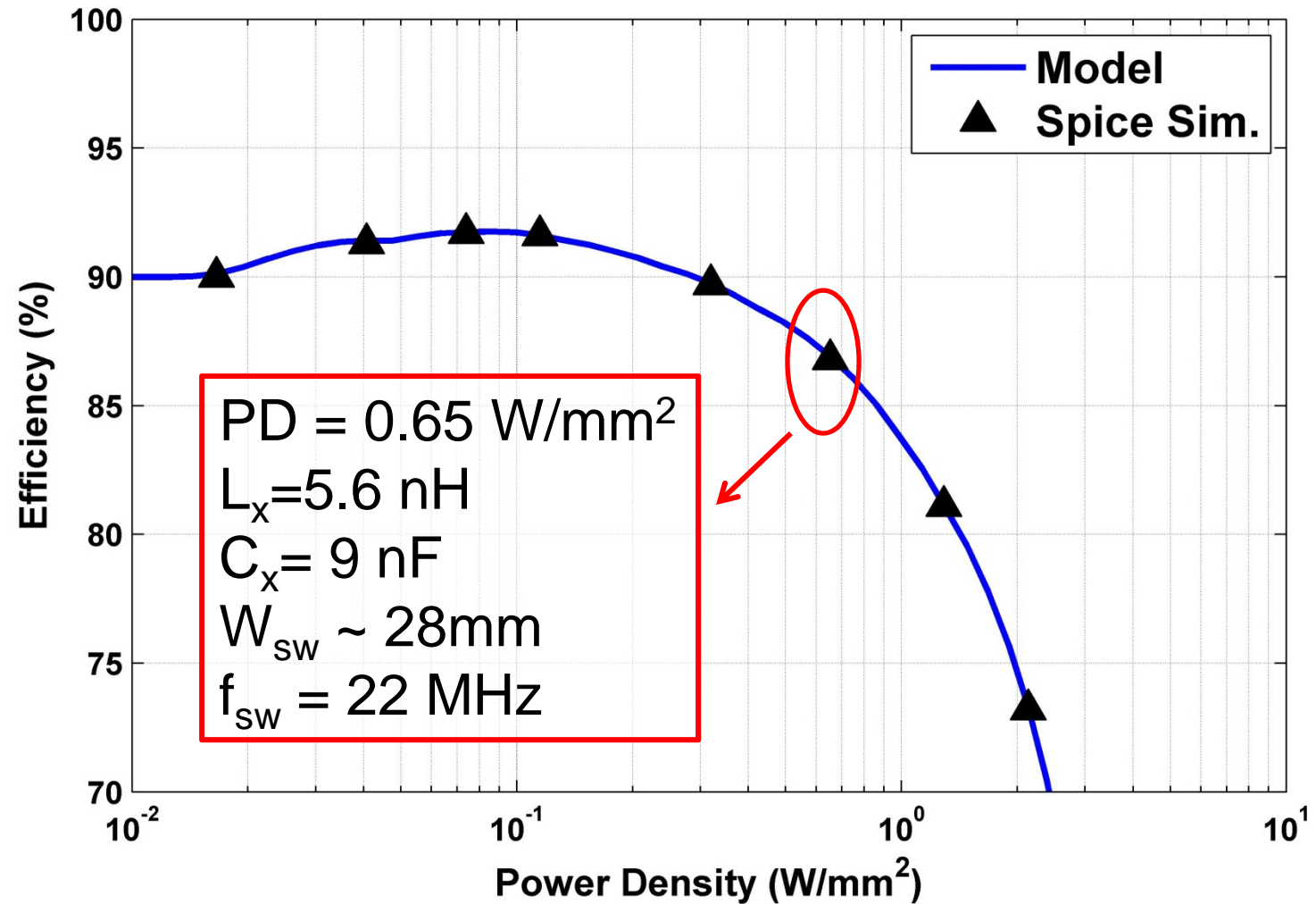
Parameter	Value
Process Technology	0.18 μm Bulk HVCMOS
Input Voltage	$\sim 6\text{ V}$
Output Voltage	$\sim 3\text{ V}$
Specific On Resistance	1.35 $\text{K}\Omega\text{-}\mu\text{m}$
Specific Input Capacitance	2 $\text{fF}/\mu\text{m}$
MIM Capacitor Density	6.6 $\text{fF}/\mu\text{m}^2$ (kbot $\sim 1\%$)
Chip Area	$< 10\text{ mm}^2$

Circuit Architecture



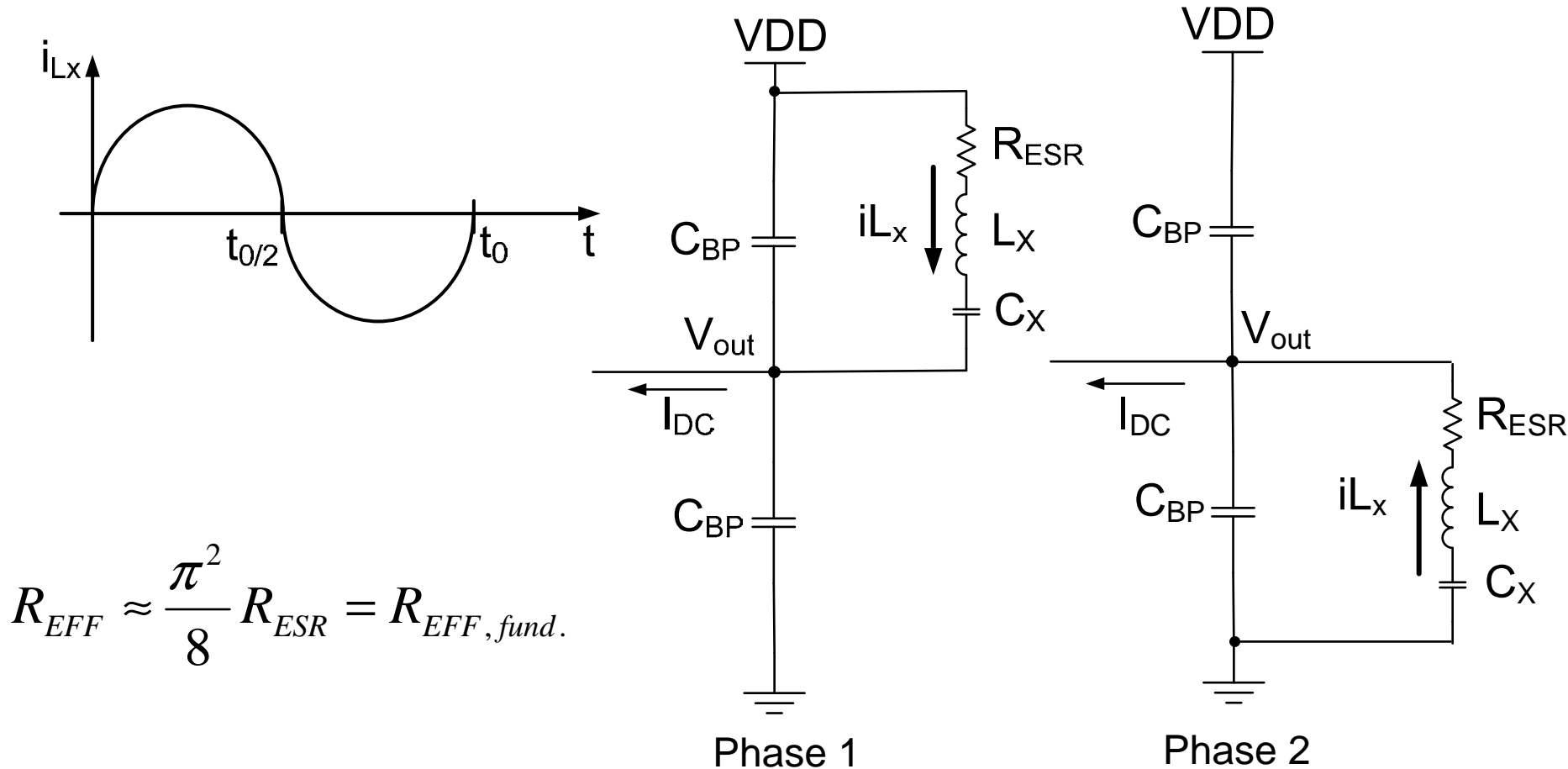
Two-phase interleaved resonant switched-capacitor (ReSC) power train for 2:1 configuration

Pareto Frontier

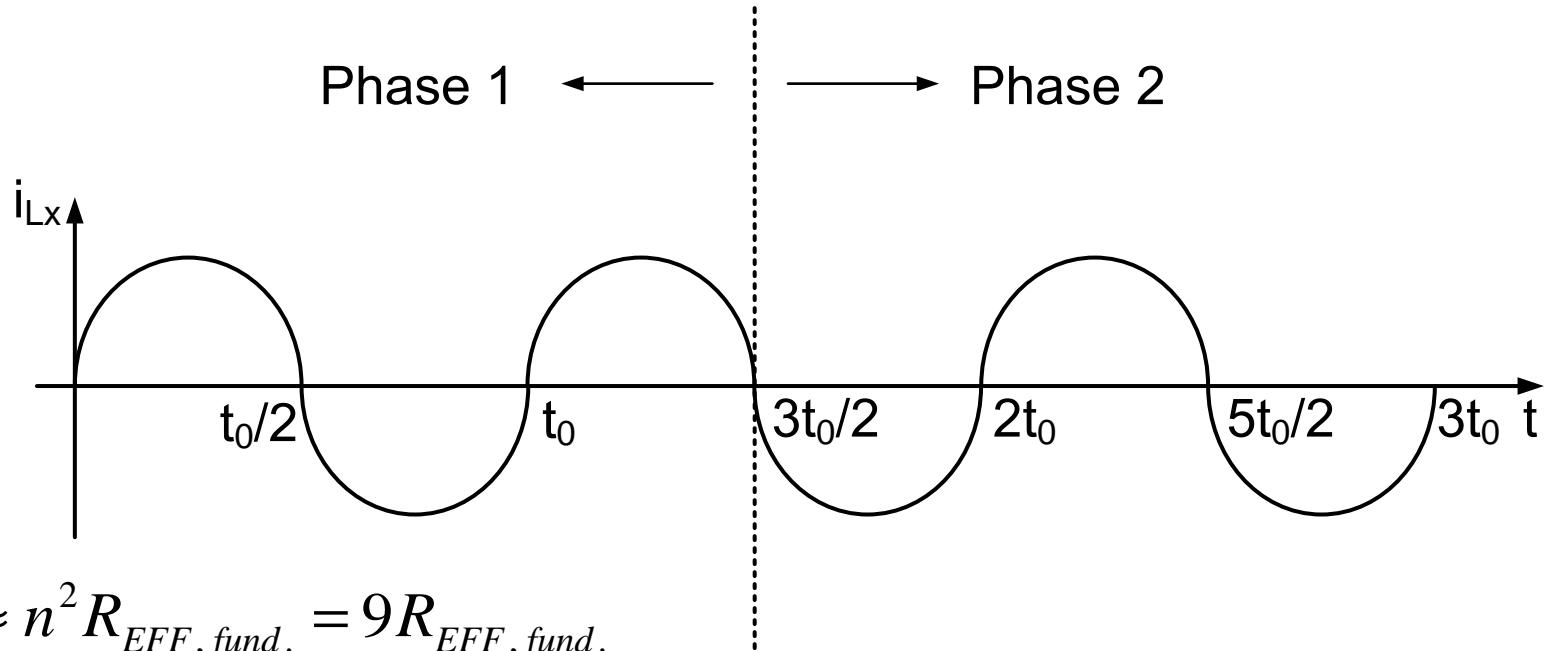


Voltage Regulation

Normal Resonant Mode



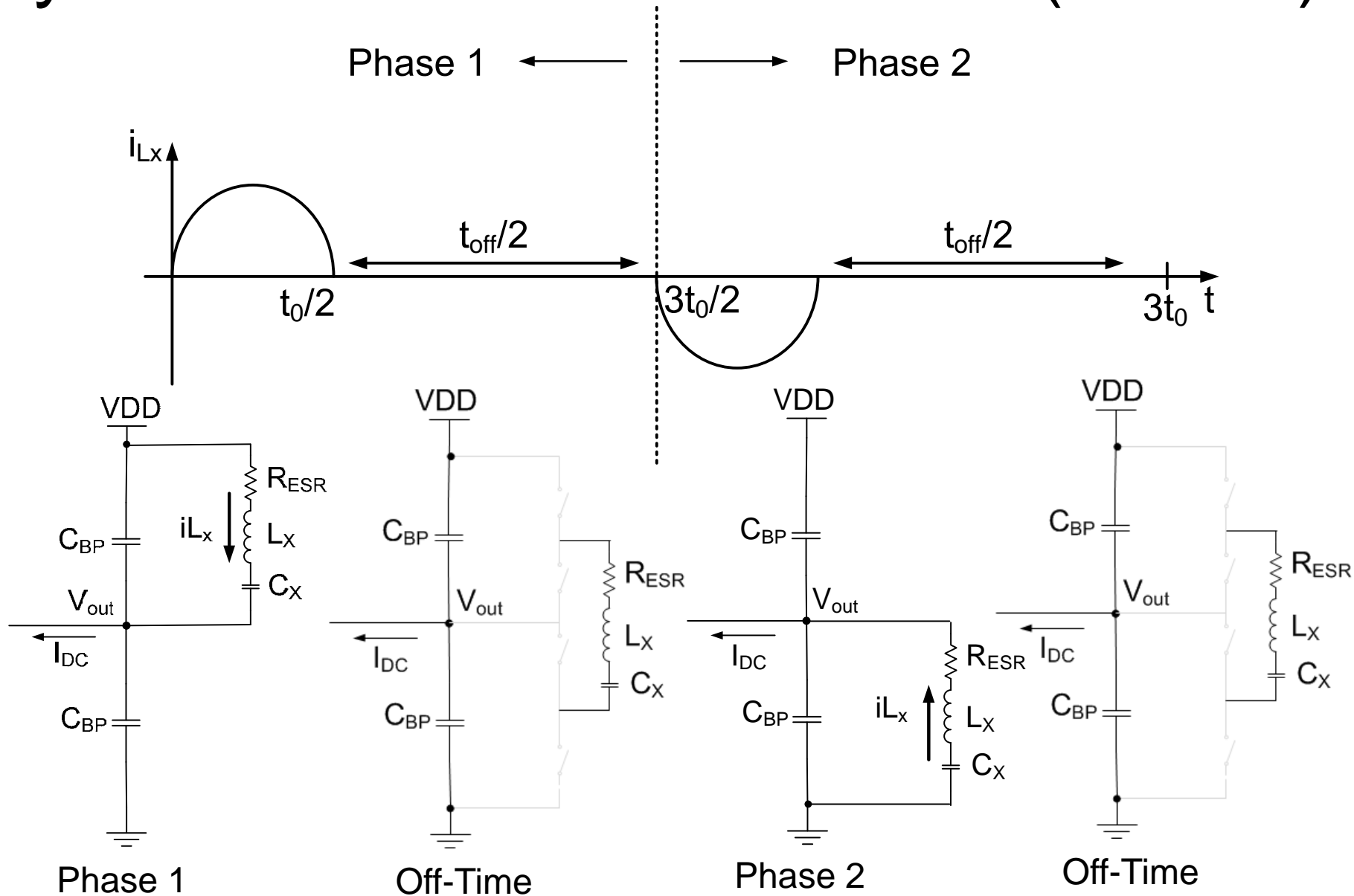
Sub-Harmonic Mode*



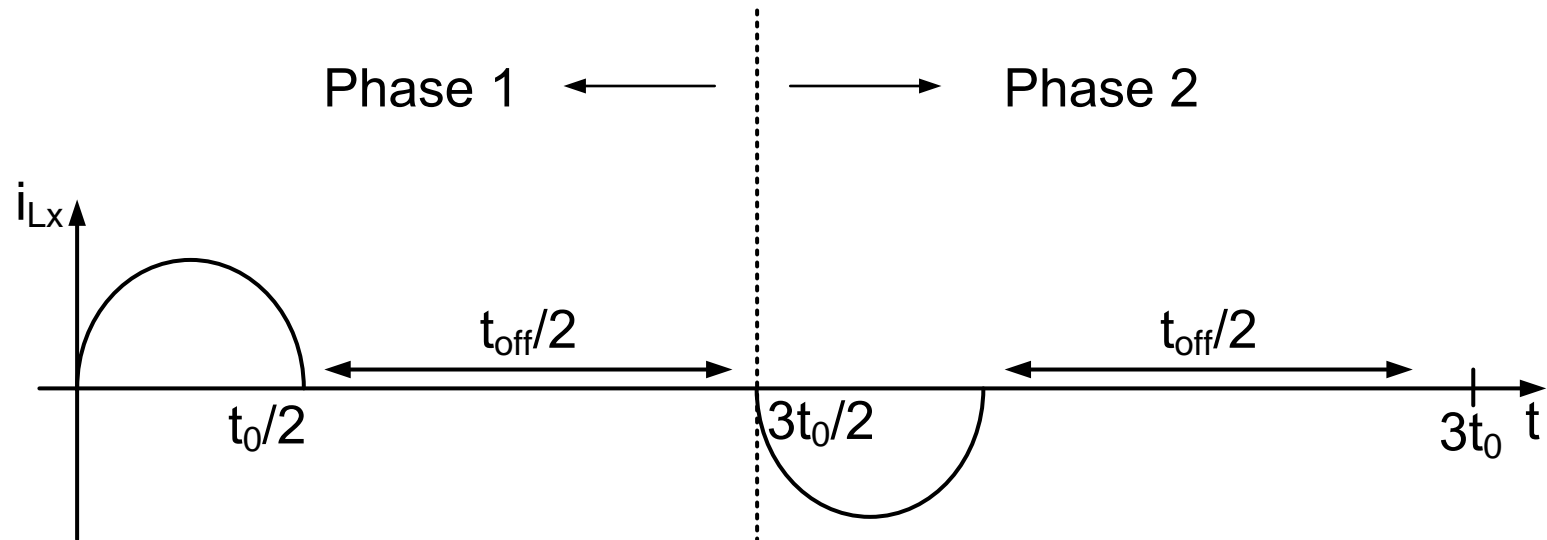
- Switching losses scale linearly
- Conduction losses scale quadratically !!
(SC converters show linear scaling with frequency)
- Overall efficiency decreases

*J.T. Stauth et. al. ISSCC 2012

Dynamic Off Time Modulation (DOTM)



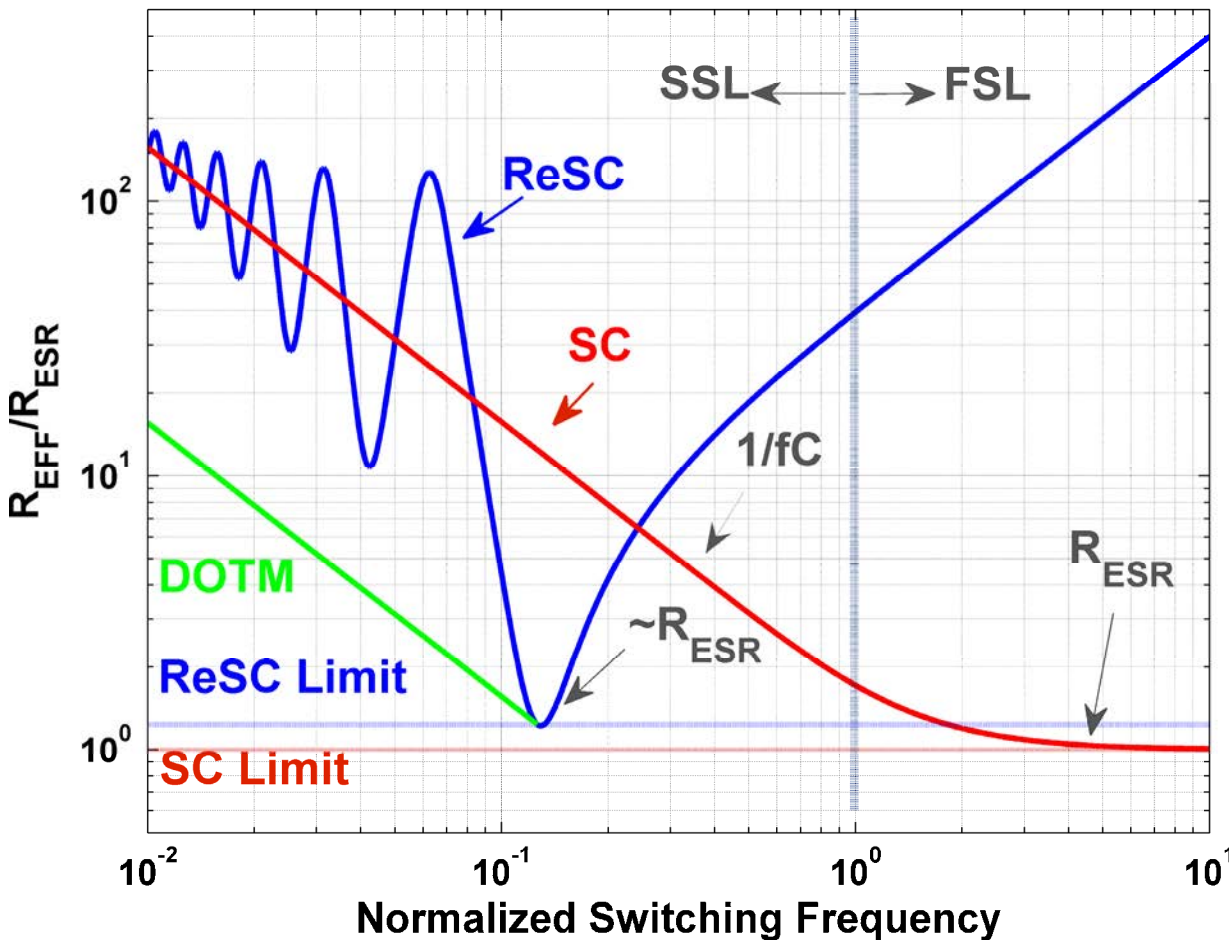
Dynamic Off Time Modulation (DOTM)



$$R_{EFF} \approx \left(1 + \frac{t_{off}}{t_0}\right) R_{EFF, fund.} = 3R_{EFF, fund.}$$

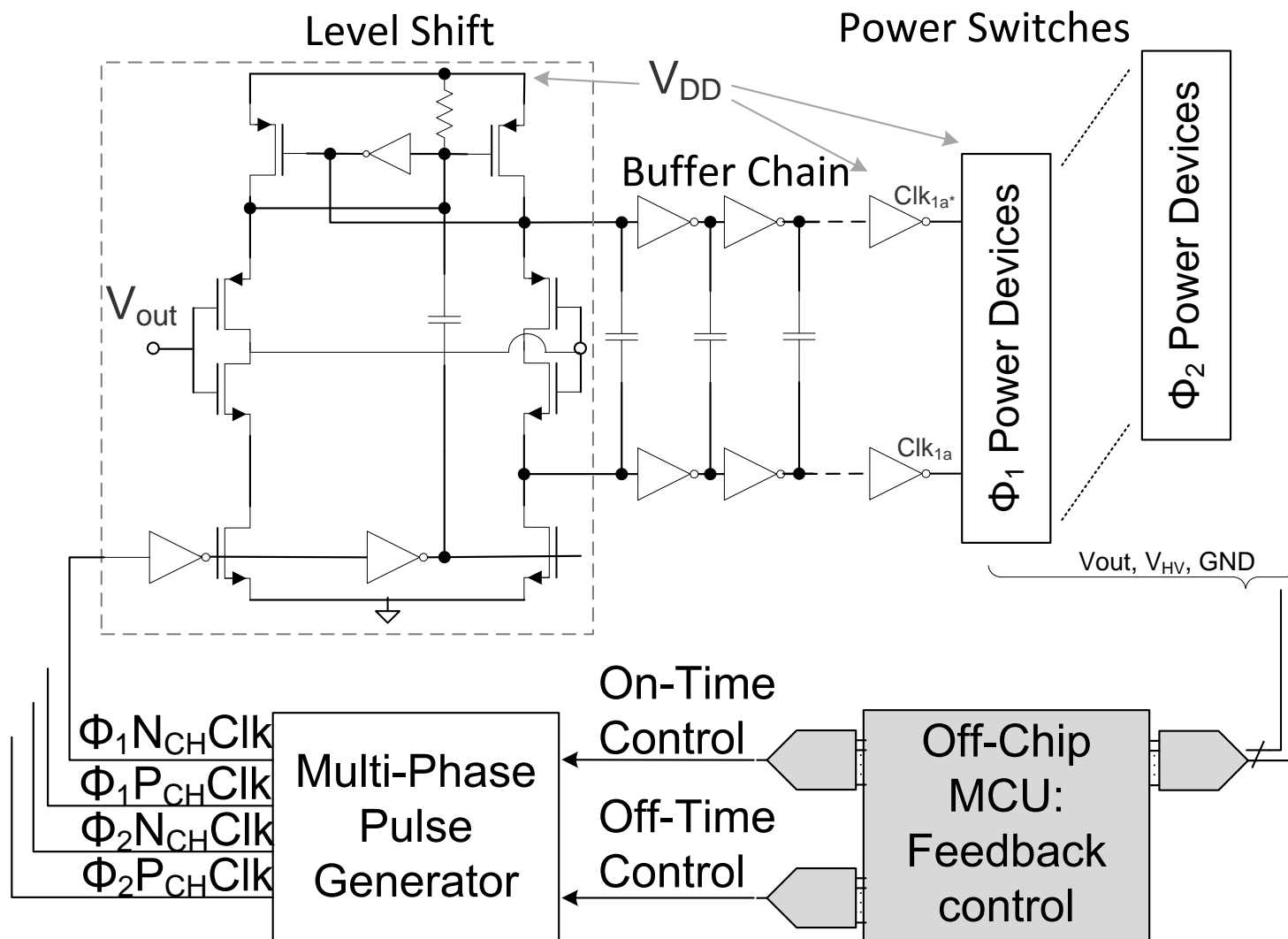
- All the switches are in high impedance for t_{off}
- Switching losses scale linearly
- Conduction losses also scale linearly
- Maintain peak efficiency in light load

Dynamic Off Time Modulation

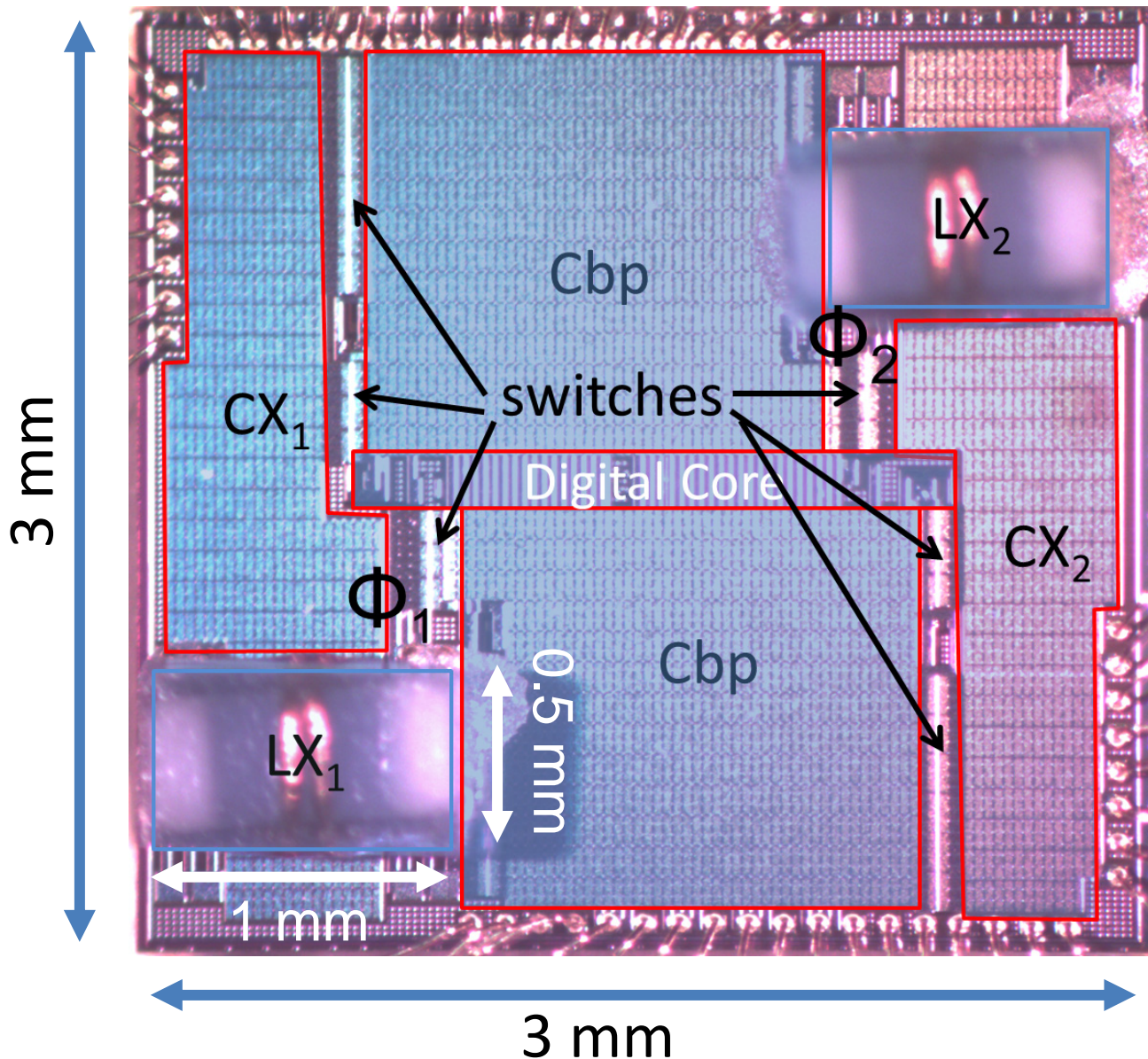


- Linear scaling of effective resistance with frequency; similar to SC converters
- Maintains peak efficiency in light-load
- Provides load-line regulation capability

IC and Embedded System

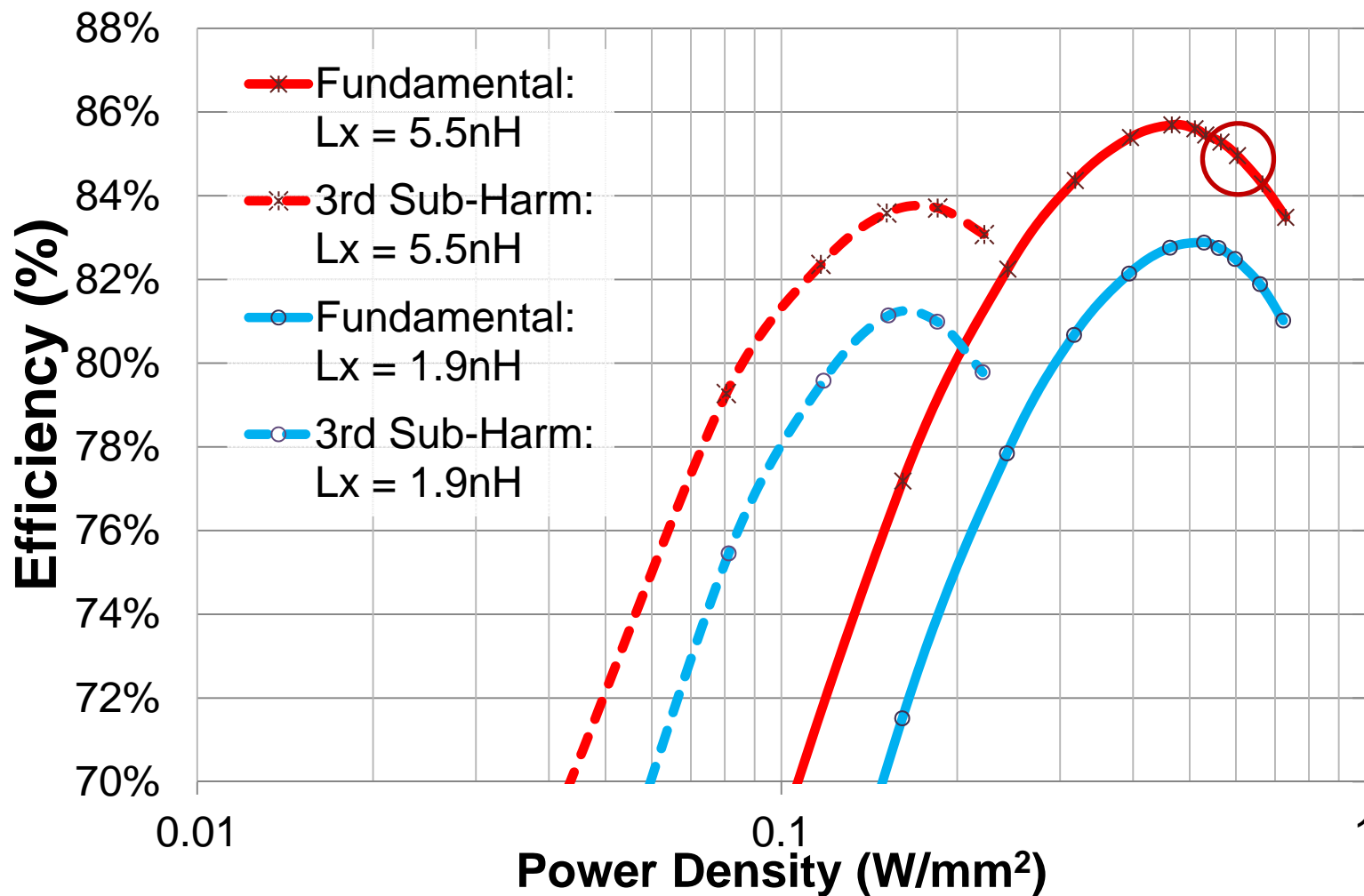


Die Photo



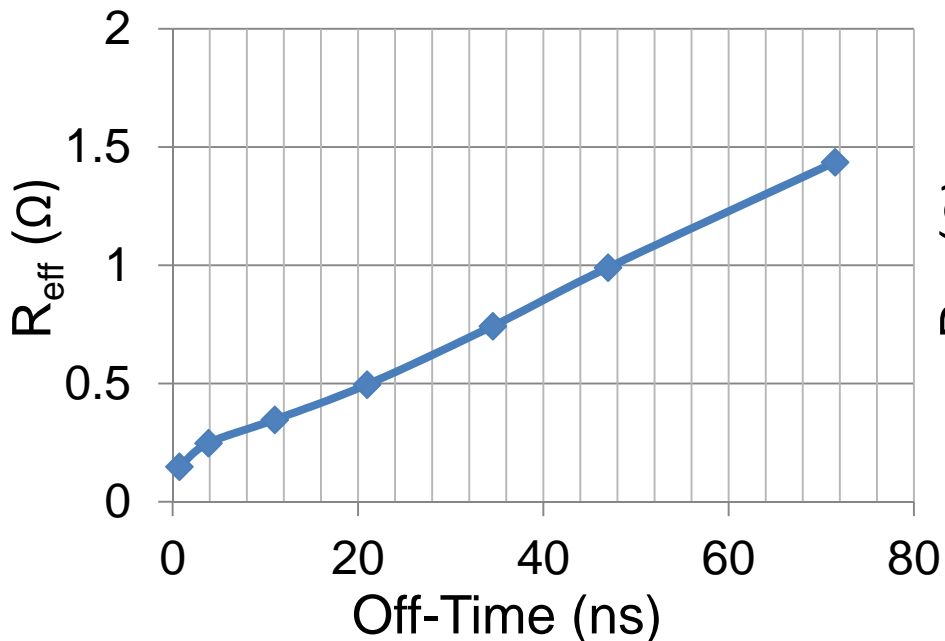
- $L_x = 1.9 \text{ nH}$
- $C_x = 9 \text{ nF}$
- $C_{bp} = 11 \text{ nF}$
- $f_{sw} = 35 \text{ MHz}$
- $0.18 \mu\text{m}$ HVCMOS

Efficiency Measurements

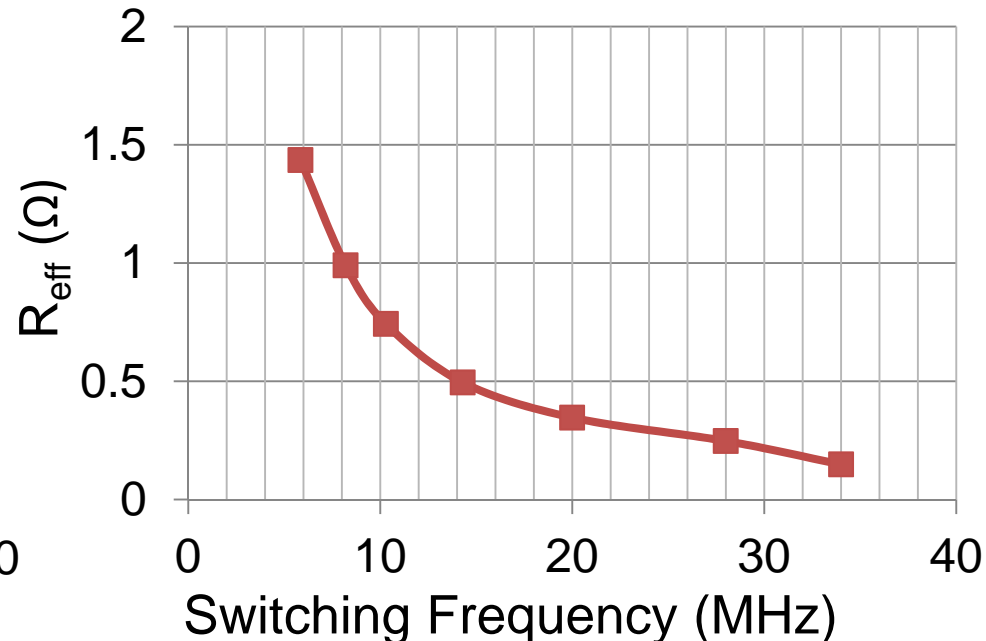


Efficiency of 85.0 % @ 0.60 W/mm^2

Dynamic Off Time Modulation

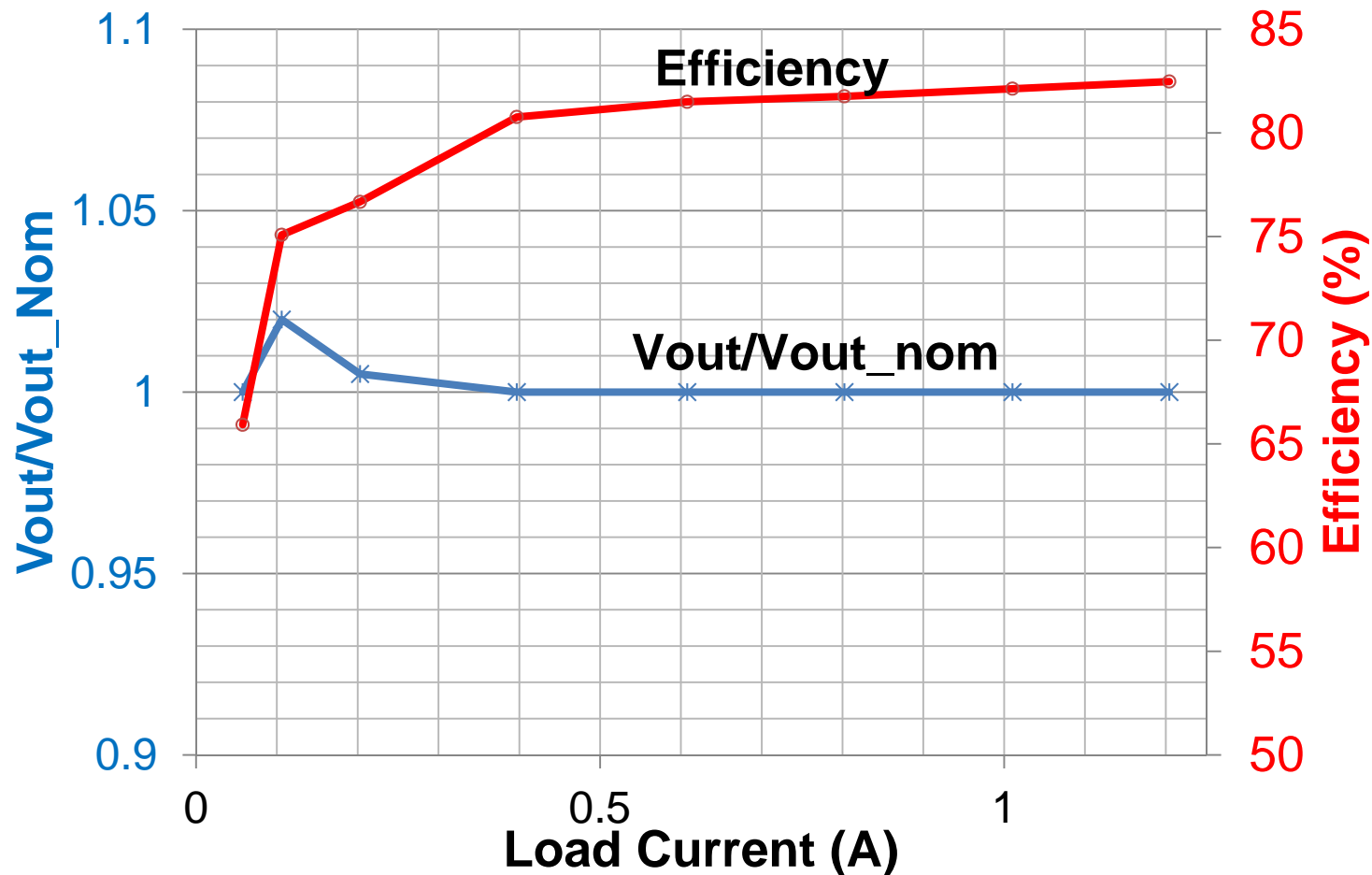


- Effective resistance increases linearly with off-time



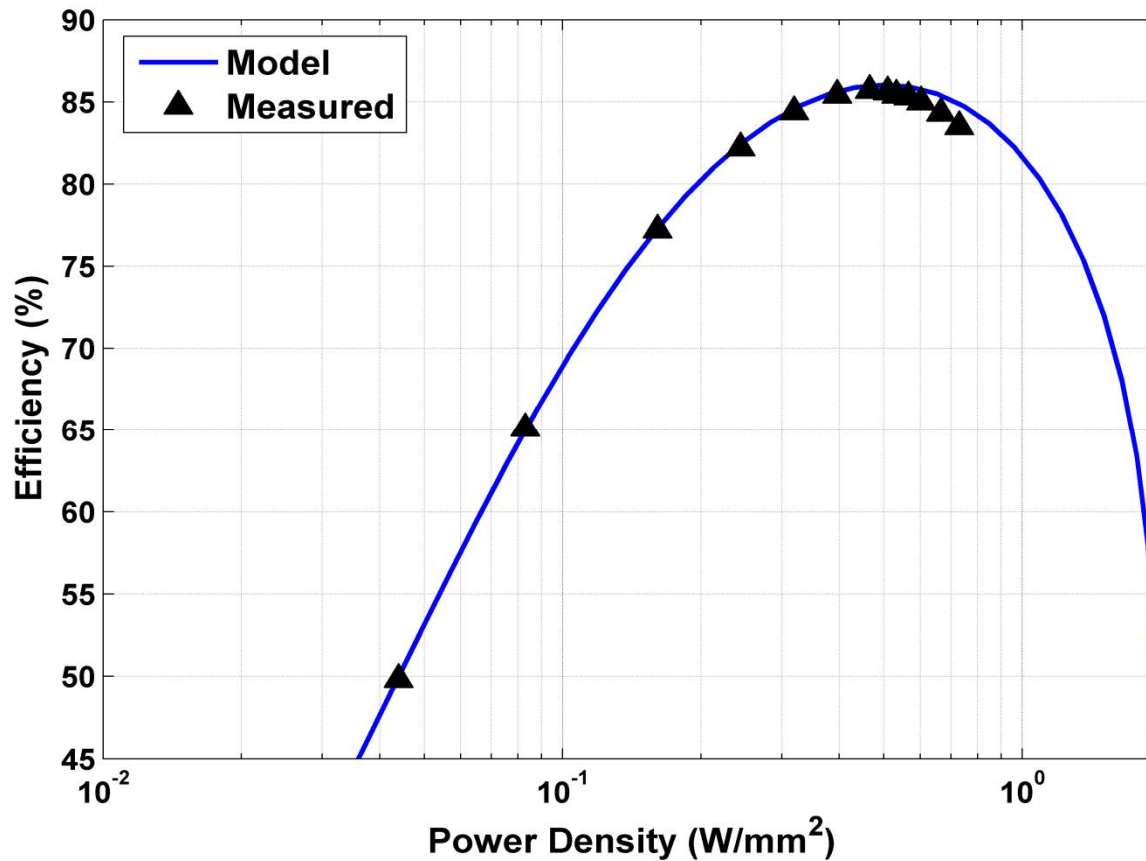
- Shows 1/f dependence; similar to SC converters

Voltage Regulation



- μC regulates the output voltage through use of DOTM
- Efficiency remains $> 80\%$ through most of the load range

Efficiency: Model vs Measurement Data

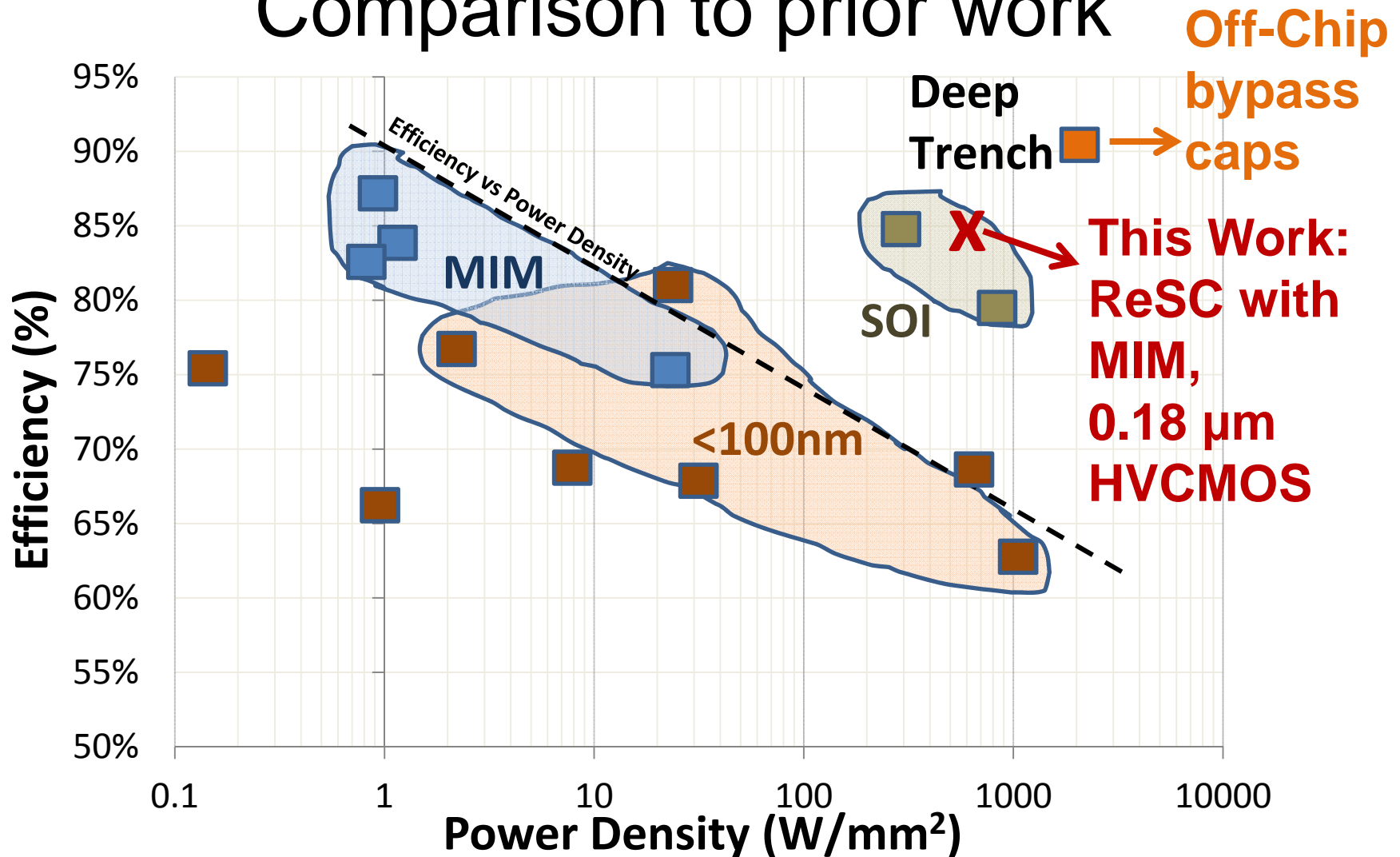


- Switch width (W_{sw}), switching inductor (L_x), flying capacitor (C_x) taken from actual design
- Only output current varied
- Reasonable agreement between the model and the measured values

Comparison to prior work

Work	ISSCC 2010	ESSCIRC 2011	COMPEL 2010	VLSI 2009	VLSI 2010	This Work
Topology	2:1, 3:2, 3:1	2:1	2:1	1:2 Step Up	2:1	2:1
Input/Output	3V/1V 2V/1V	2V/1V	3.6V/1.5V	1V/2V	2V/1V	6V/3V 2.7V/1.35V
Capacitor Technology	MOS	MOS	MIM	MIM	Deep Trench	MIM
Process Technology	32nm SOI	90nm bulk CMOS	90nm bulk CMOS	130nm bulk CMOS	45nm SOI	0.18 μ m bulk HVCMOS
Interleaved Phases	32	21	1	16	1	2
Power Density (PD)	0.86 W/mm ²	0.77 W/mm ²	0.046 W/mm ²	0.067 W/mm ²	2.185 W/mm ²	0.6 W/mm ²
Efficiency @ PD	79.76%	69%	74%	82%	90%	85%
Maximum Output Power	0.325 W	1.65 W	0.150 W	0.151 W	2.62 W	4.32 W

Comparison to prior work



G.V. Pique et. al., IEEE TPEL 2013

Conclusions

- Need for fully-integrated power management supporting future digital integration.
- ReSC converters offer performance advantages compared to SC architectures; positioned to leverage future integrated magnetic components
- Demonstrated 2 phase 2:1 ReSC converter with 85% efficiency @ 0.6 W/mm²
- Demonstrated a technique (DOTM) for providing load-line regulation capability for ReSC converter; similar to SC converter

Acknowledgement



THAYER SCHOOL OF
ENGINEERING
AT DARTMOUTH



Thayer School of Engineering, Dartmouth College



National Science Foundation
(Award No. 1309905)

Thank You!

An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched- Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

Loai G. Salem and Patrick P. Mercier
University of California, San Diego

ISSCC 2014

Parallelism, The Way For Higher Processing

- Higher-frequency exceeds thermal limits

High performance & low power:

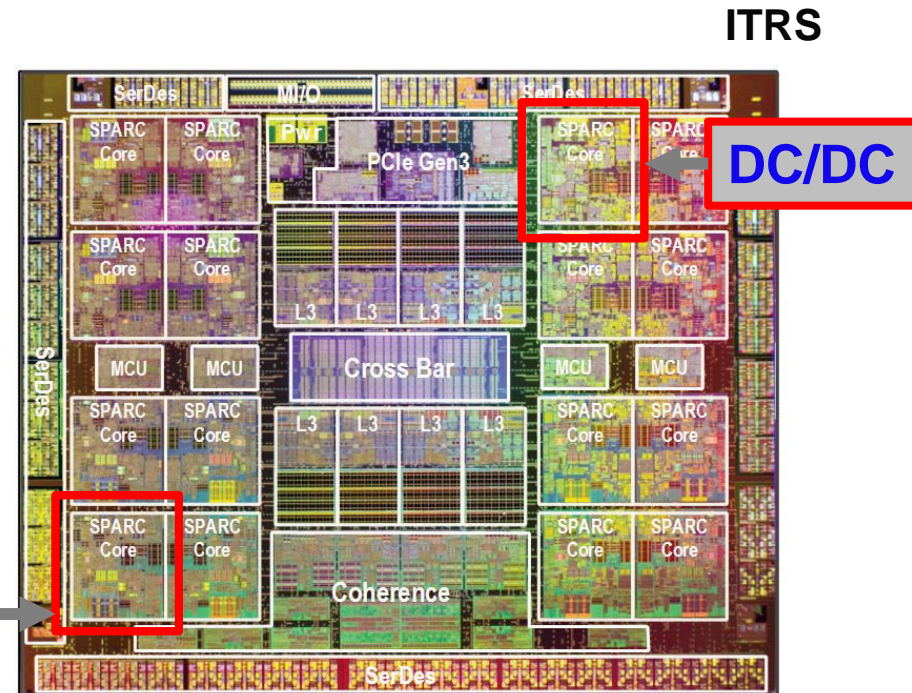
- Parallel processing (multi-core)

No. of processing engines exponentially increases to meet customer expectations

Per-module voltage scaling for adapting power with processing load

Fully-integrated DC-DC Converters are required

DC/DC



T5 SPARC, 16 Core, ISSCC'13

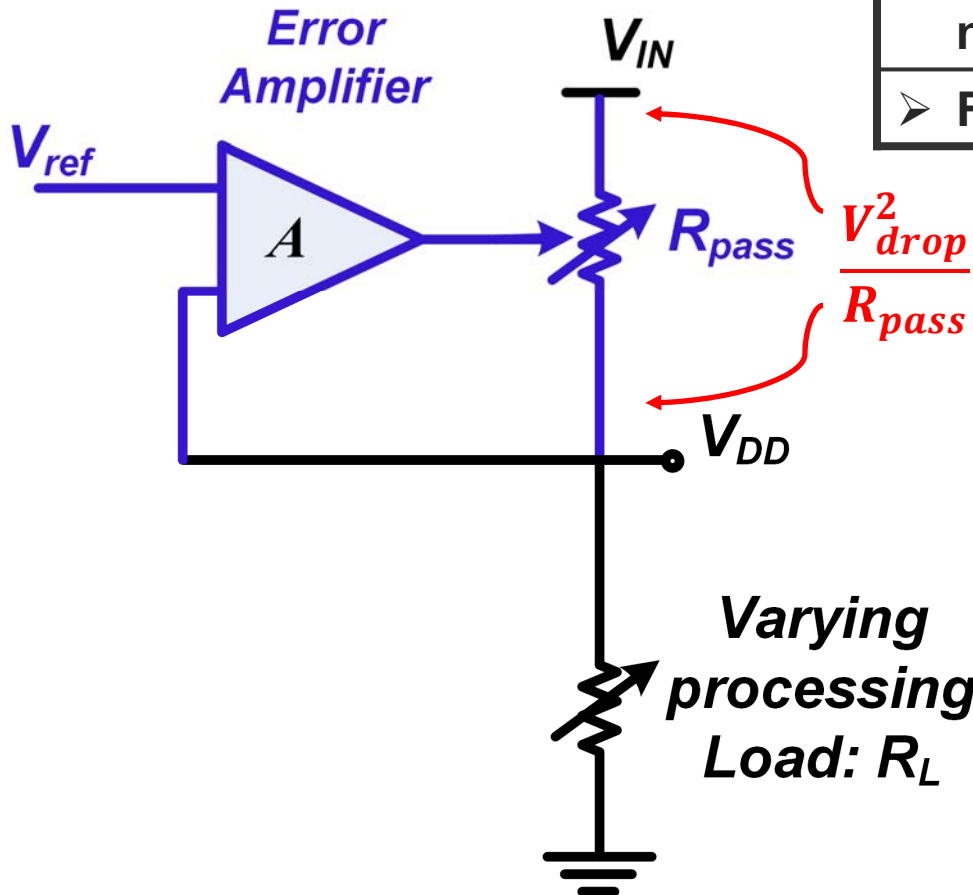
4.6: An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

Outline

- **On-Die DC-DC Converters**
- **Recursive SC Topology**
- **All Digital Binary Search Control**
- **Measurement Results**
- **Conclusions**

Linear Voltage Regulator

- A resistive divider



➤ Compact

➤ No switching noise

➤ Fast

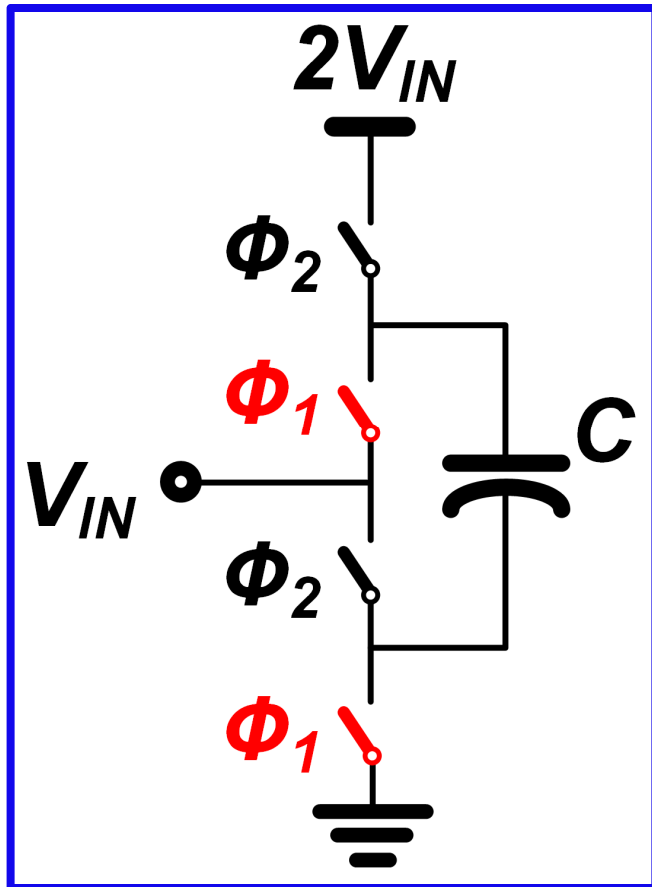
➤ **Very lossy** when V_{DD} goes far below V_{IN}

$$\eta = \frac{V_{DD}}{V_{IN}}$$

Switching DC-DC Converters

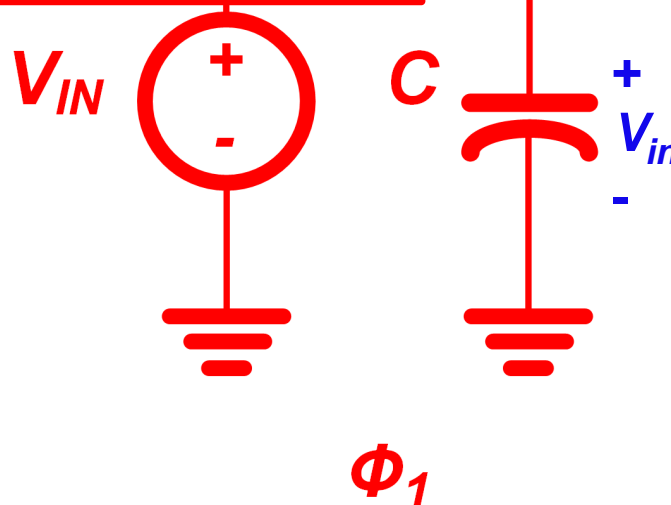
- How to convert input DC voltage?

Switched Capacitor



Switched Inductor

Continuous Conversion by duty cycle



Low-Pass Filter

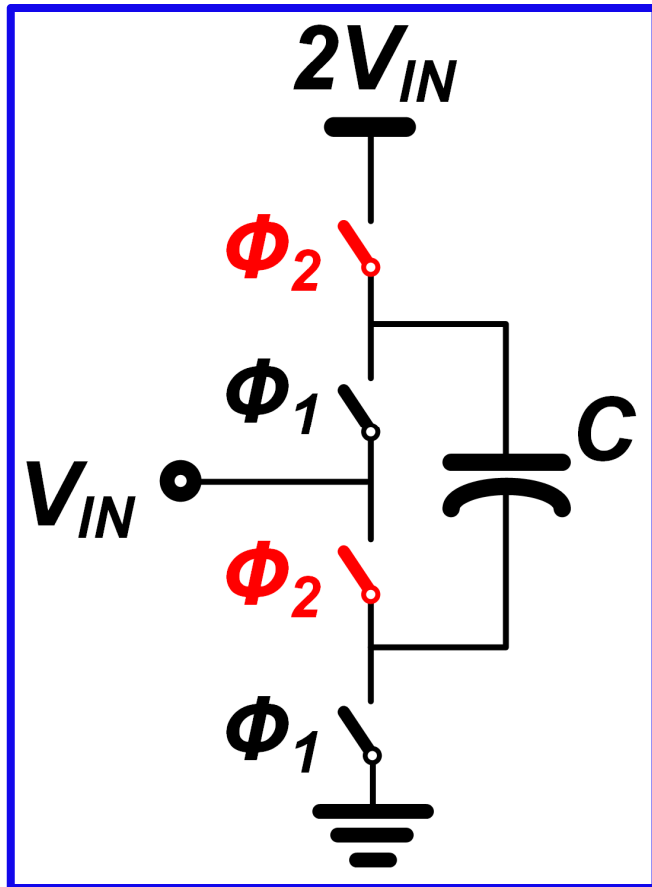
Fourier Series of a Square Signal

DC f_{sw} $3f_{sw}$ f

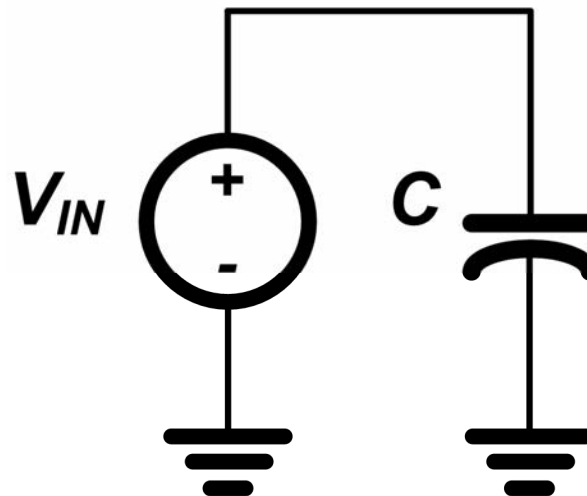
Switched Capacitor DC-DC Converters

- How to convert input DC voltage?

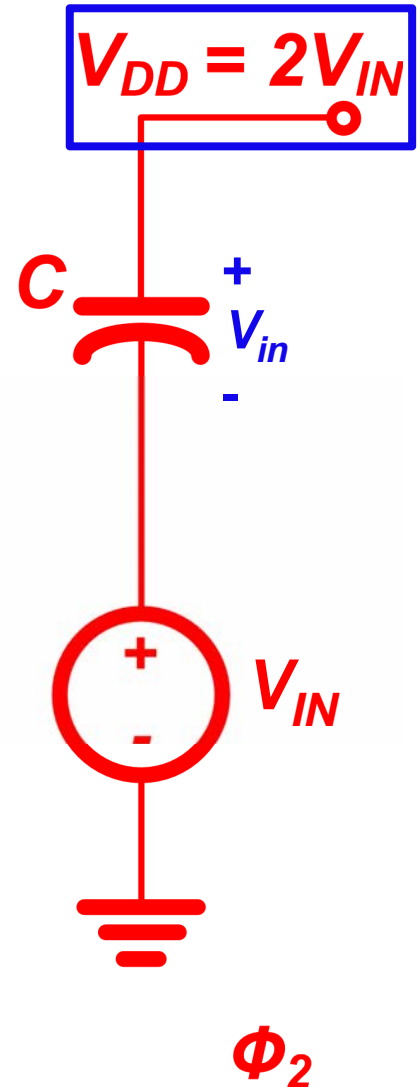
Switched Capacitor



*Voltage doubler
fixed 1:2 conversion*



Φ_1

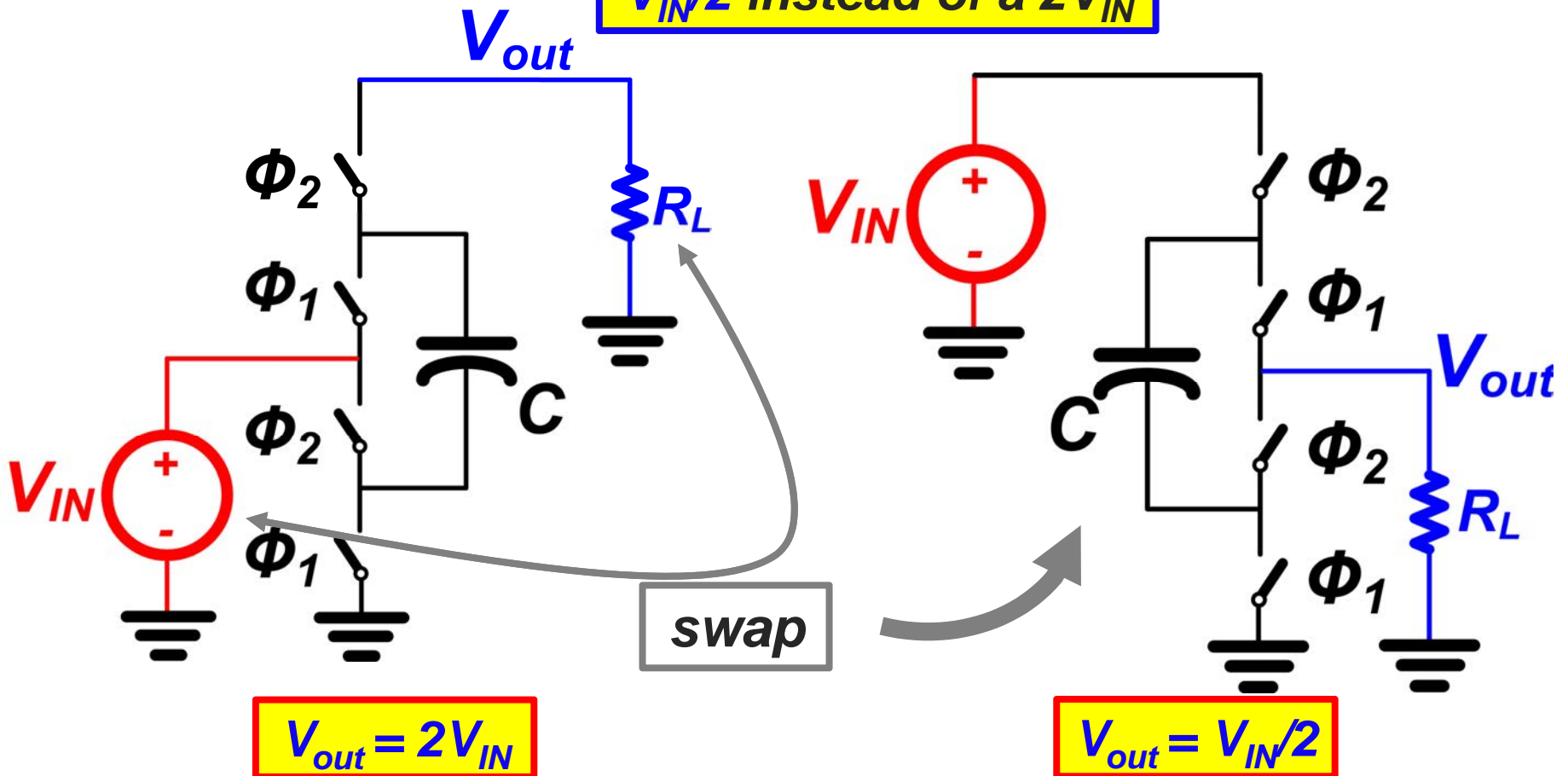


Φ_2

Switched Capacitor DC-DC Converters

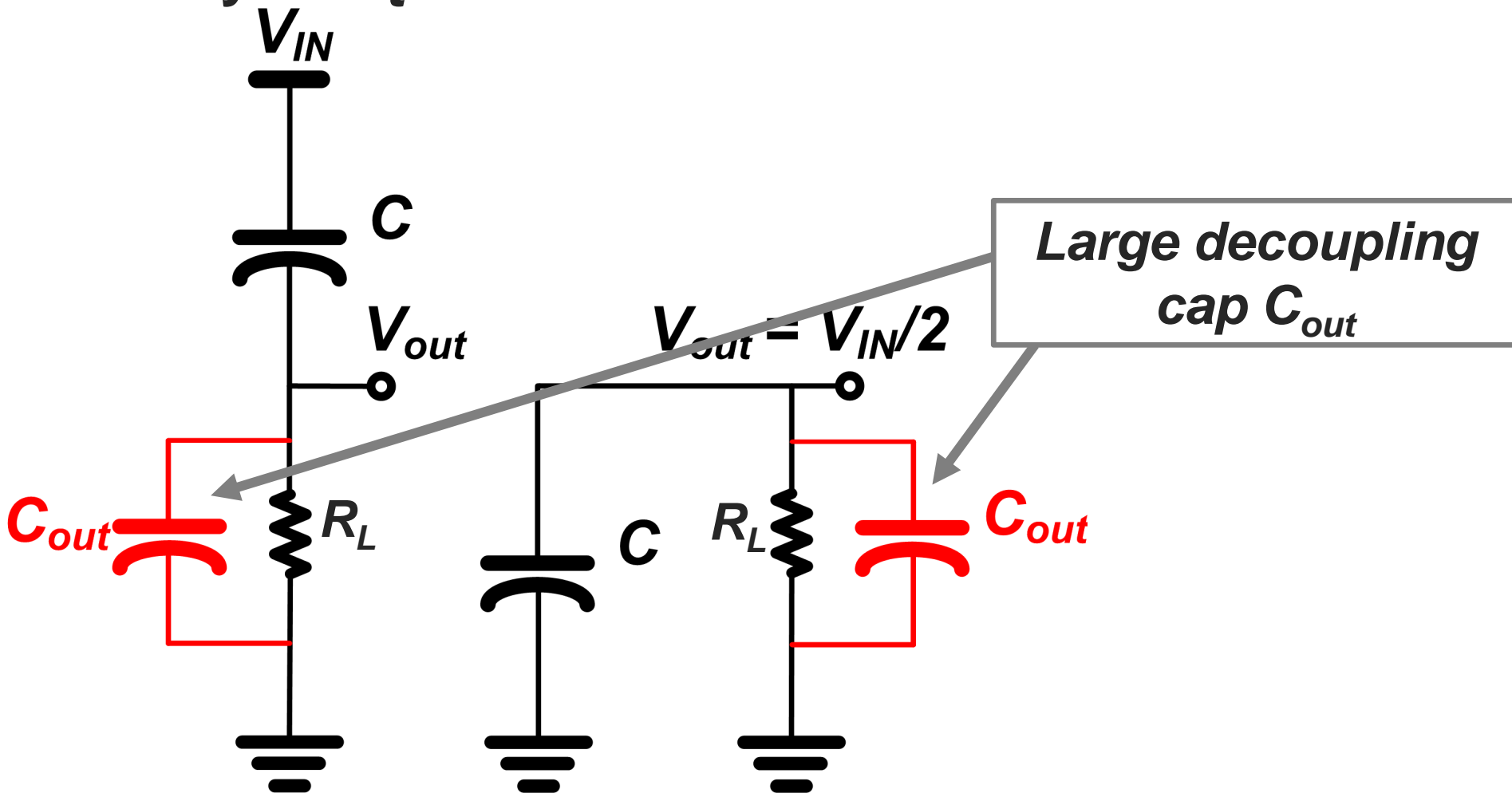
- How to convert input DC voltage?

Swap V_{IN} and R_L for $V_{IN}/2$ instead of a $2V_{IN}$



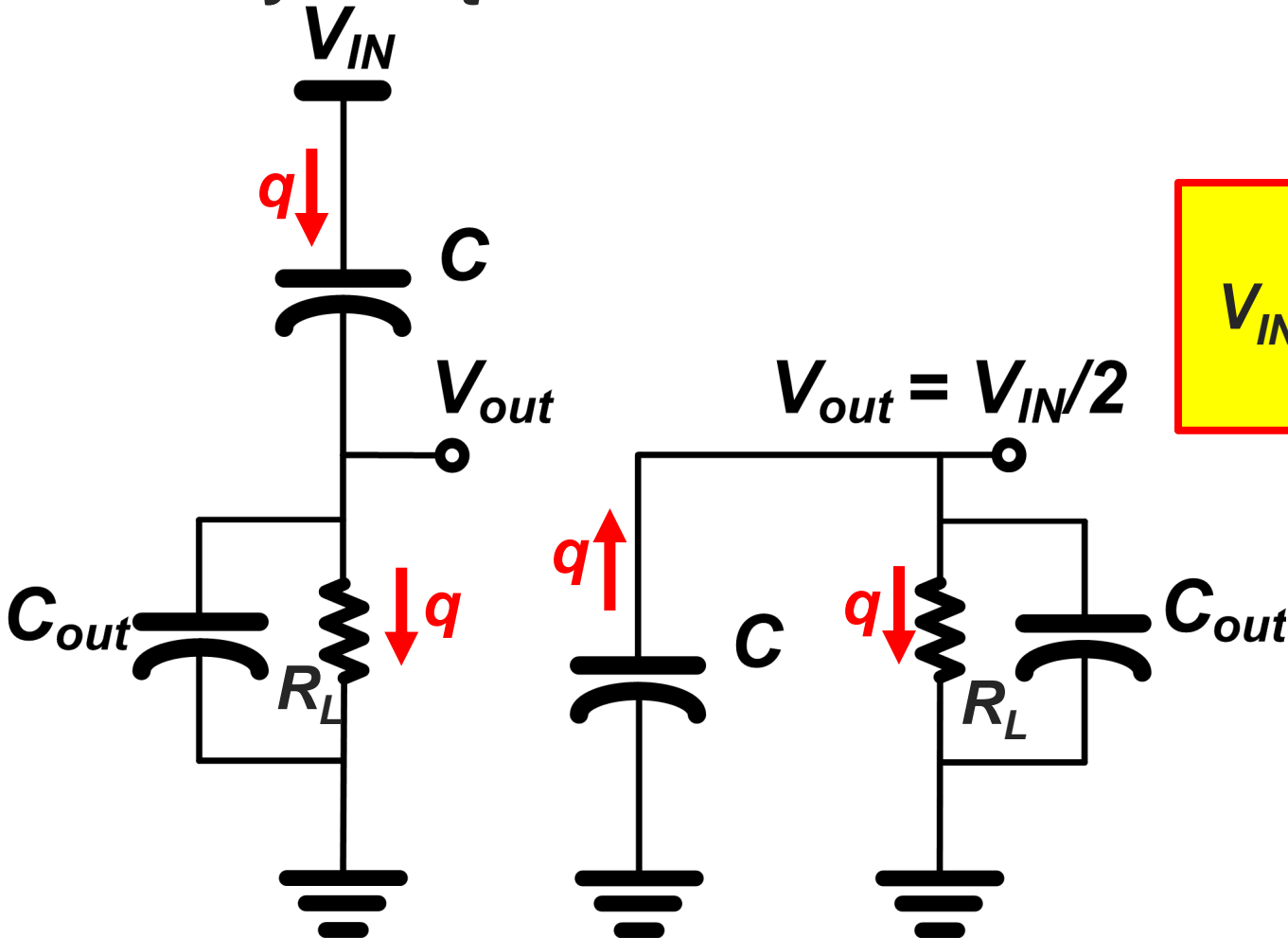
SC Loss

- Why SC $\eta \neq 100\%$?



SC Loss

- Why SC $\eta \neq 100\%$?



$$q_{out} = 2q$$

$$V_{IN} q = V_{IN}/2 \cdot 2q$$

$$E_{in} = E_{out}$$

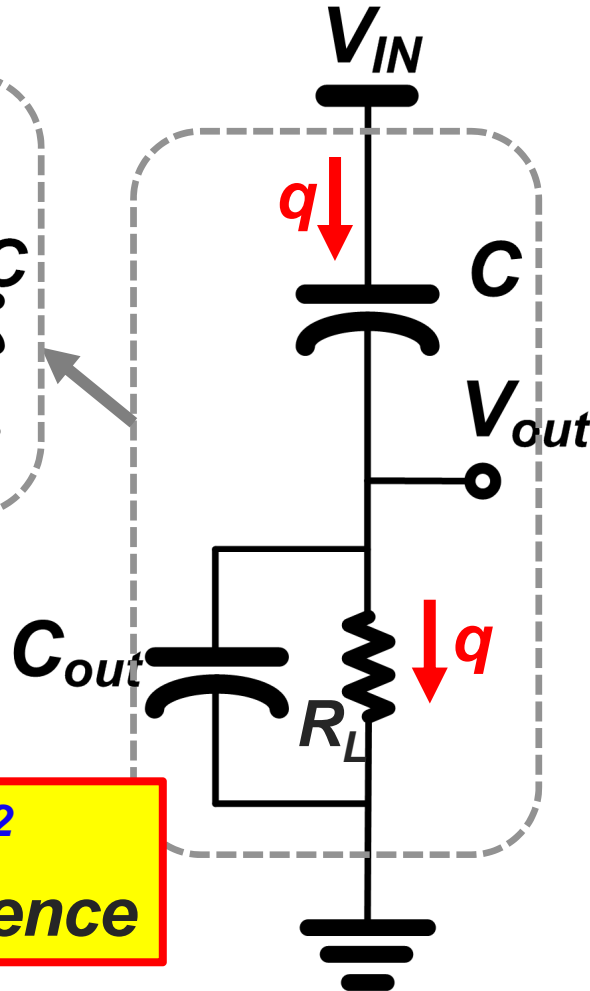
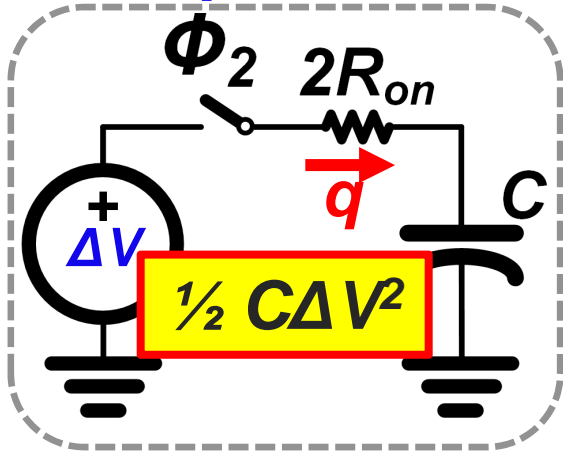
Charging

discharging

SC Loss

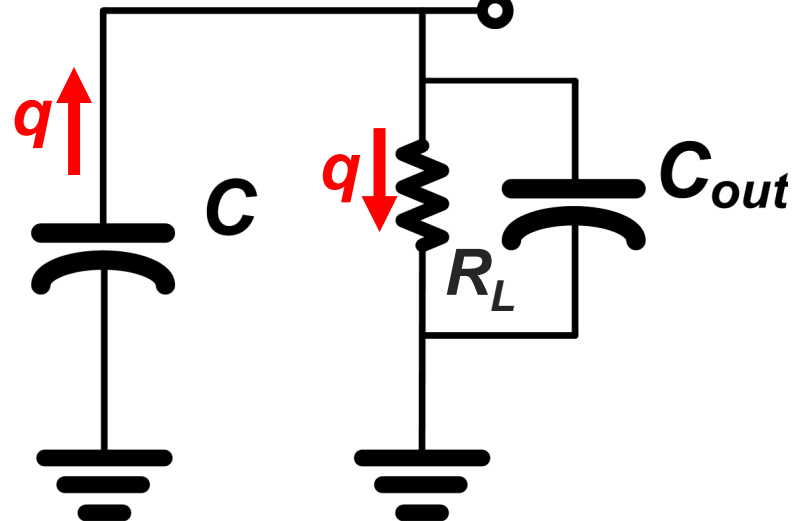
- Why SC $\eta \neq 100\%$?

Equivalent



$$\begin{aligned} f_{sw} \uparrow &\Rightarrow \Delta V \downarrow \\ C \uparrow &\Rightarrow \Delta V \downarrow \end{aligned}$$

f_{sw} $V_{out} = V_{IN}/2$



$$E_{loss} = C \Delta V^2$$

No R_{on} dependence

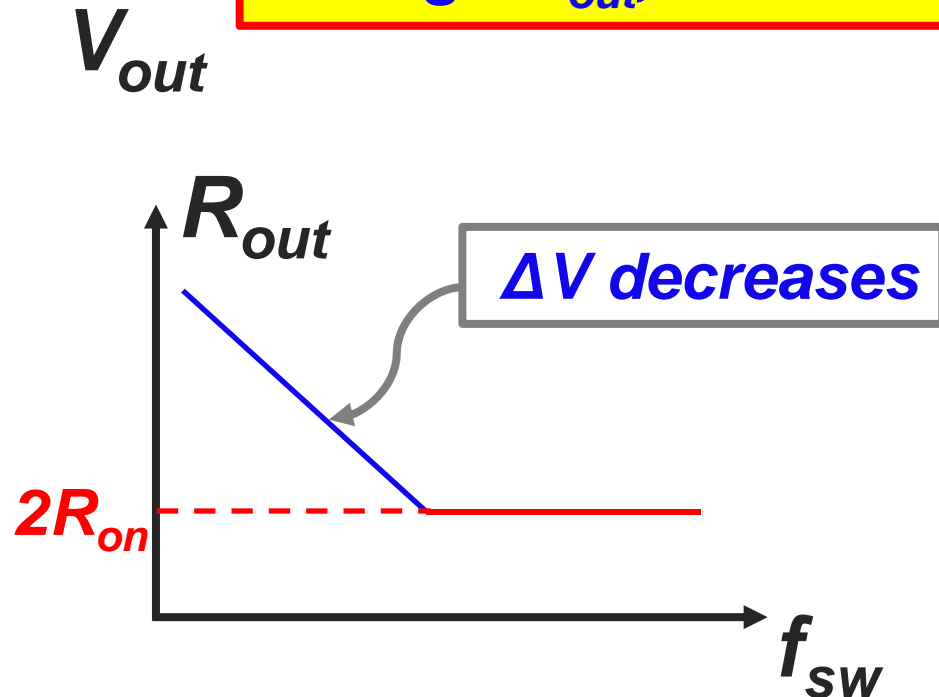
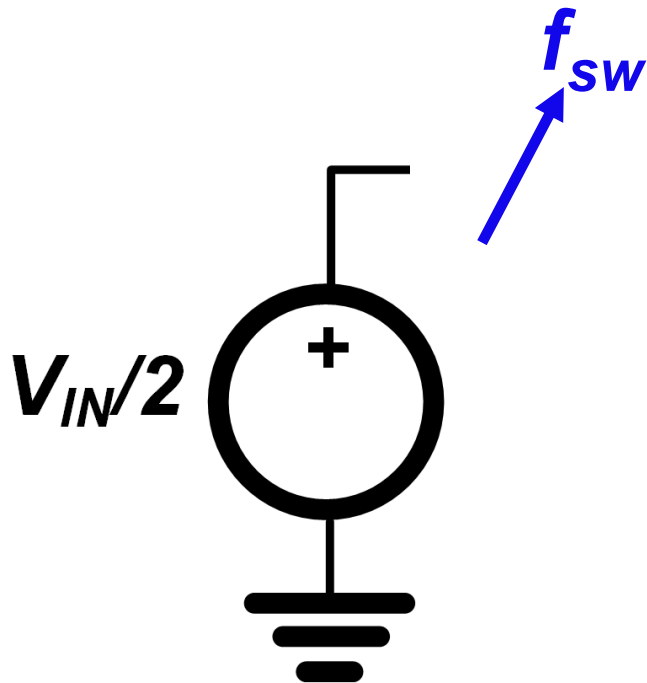
Charging

discharging

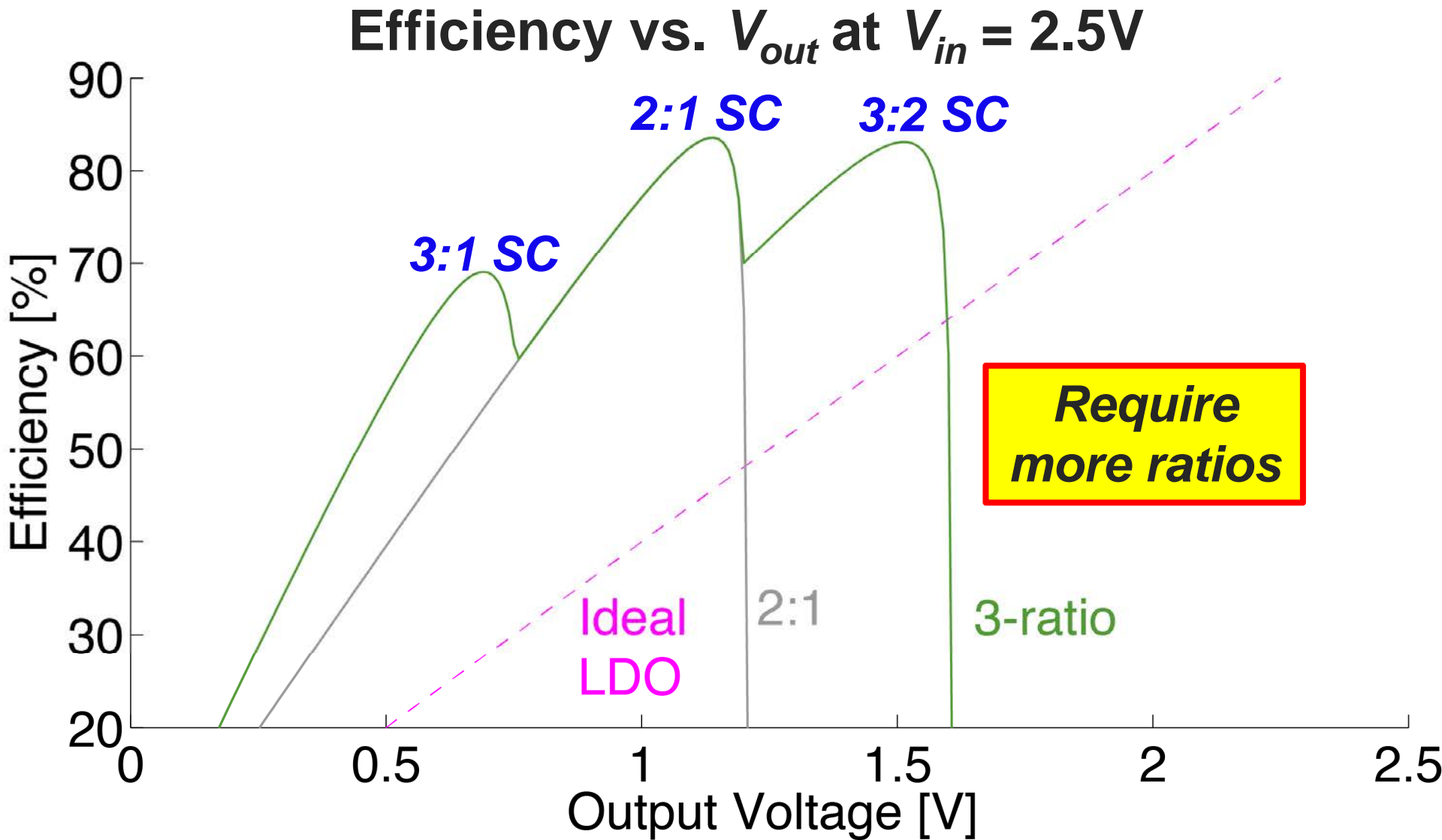
2:1 SC Model

- Loss can be modeled by R_{out}

This is how to provide continuous conversion: change R_{out} like an LDO

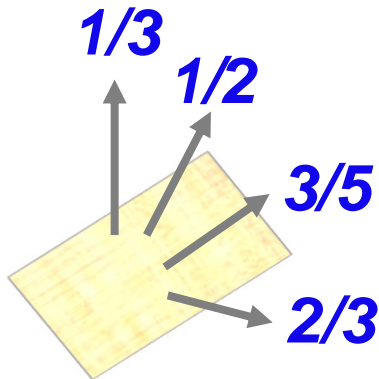


Series-Parallel SC Efficiency



Higher Number of Ratios Challenge with Conventional SC Topologies

Problem: Given certain C, re-use that to produce different ratios



- *No. Of caps and switches increases exponentially*
- *Each ratio requires a unique **arrangement**, which is difficult to re-use among other ratios*

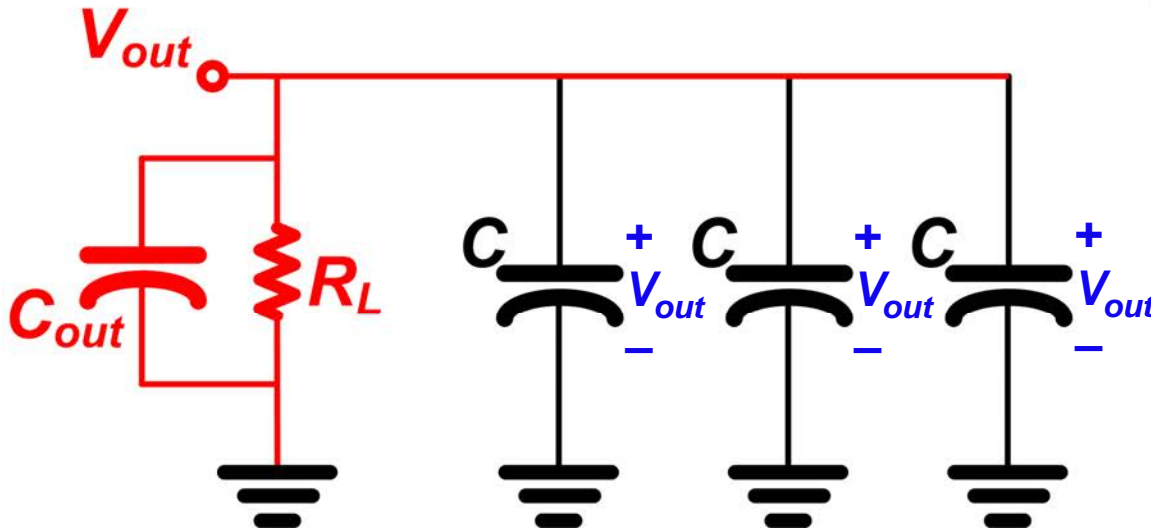
*Higher no. of ratios requires a **Modular topology***

SC 4:1 Series-Parallel

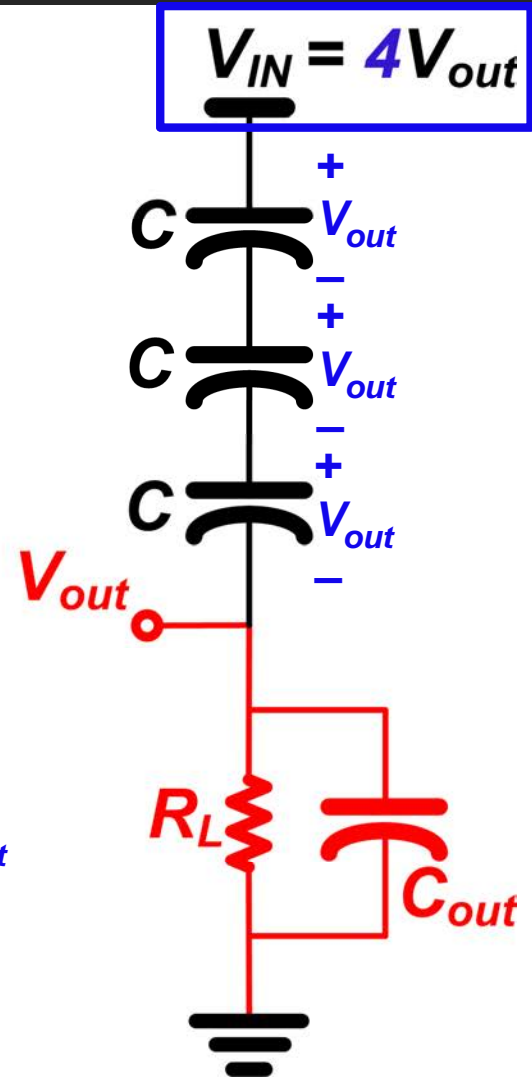
- Conventional 4:1

$$V_{out} = V_{IN}/4$$

Cap no.	3
SW no.	10



Parallel

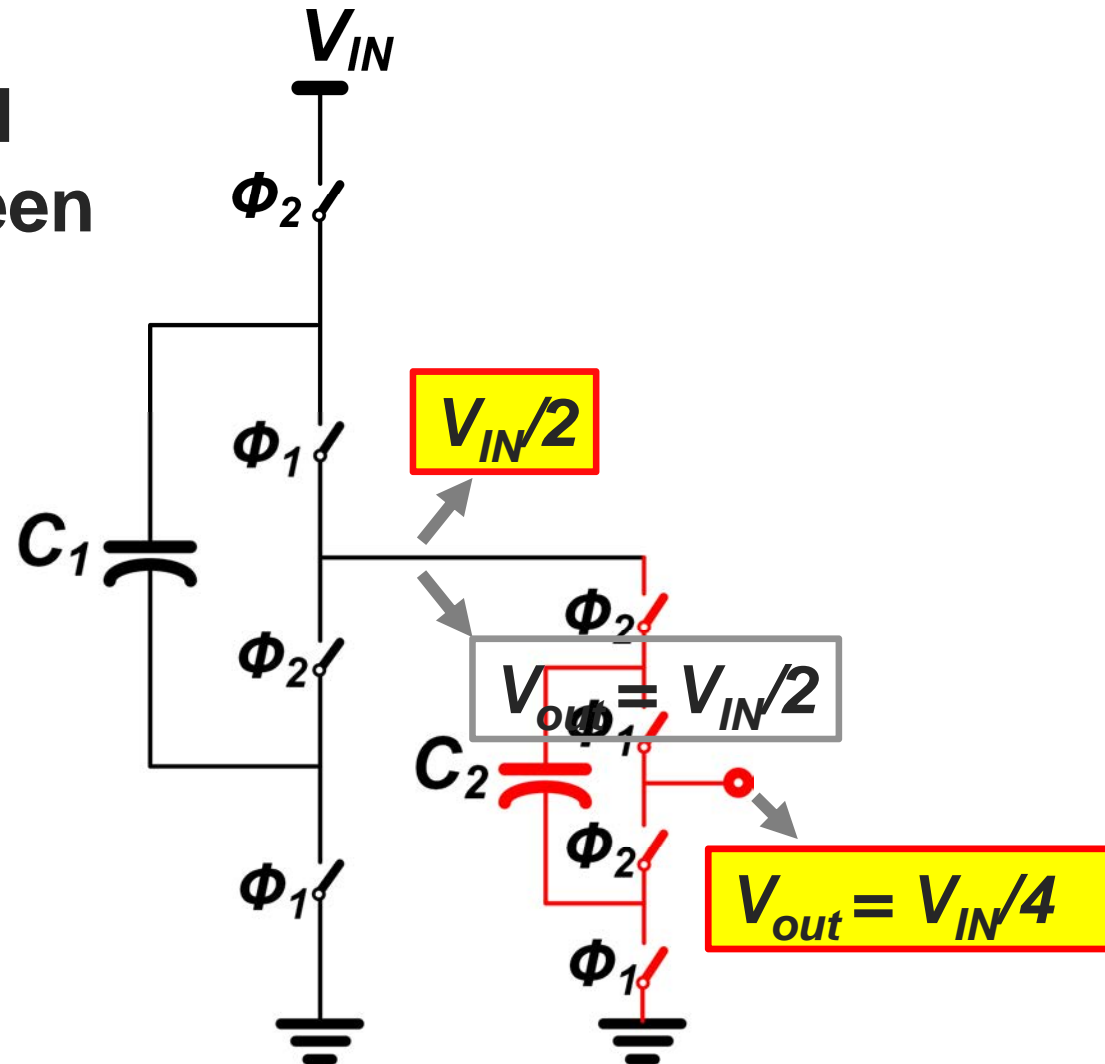


Series

Proposed Modular Switched-Capacitor Topology

- **Ratio = 1/4**
- Connect a second 2:1 cell (C_2) between cell (C_1) output & GND

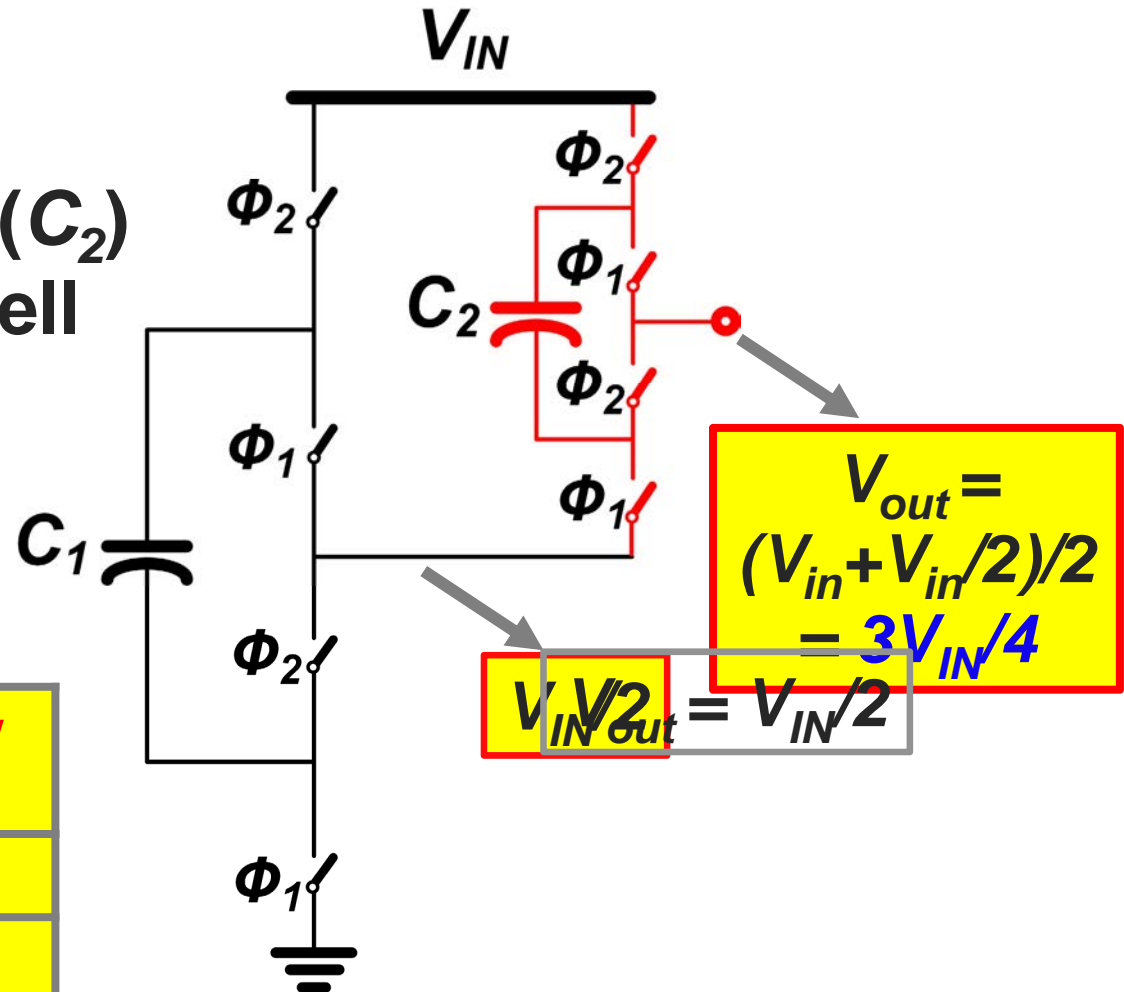
	SP 1/4	New 1/4
Cap no.	3	2
SW no.	10	8



Proposed Modular Switched-Capacitor Topology

- **Ratio = 3/4**
- Connect the second 2:1 cell (C_2) between V_{IN} & cell (C_1) output

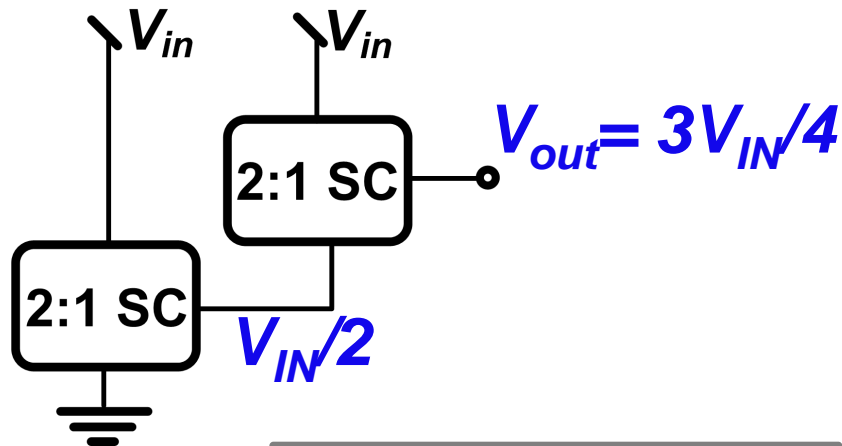
	SP 3/4	New 3/4
Cap no.	3	2
SW no.	10	8



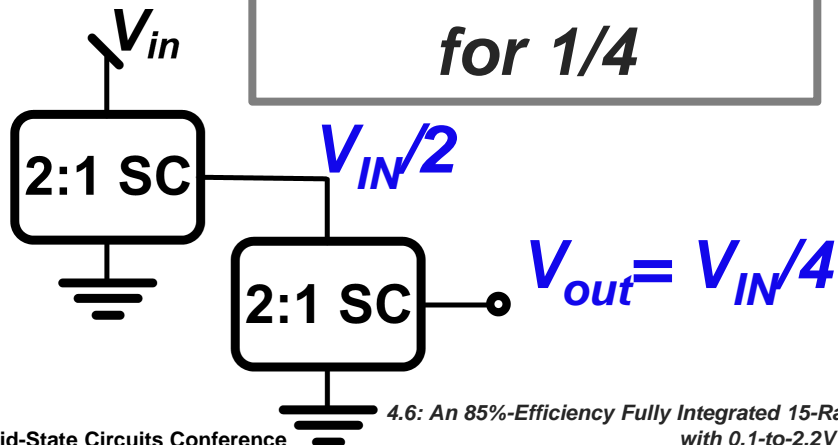
SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

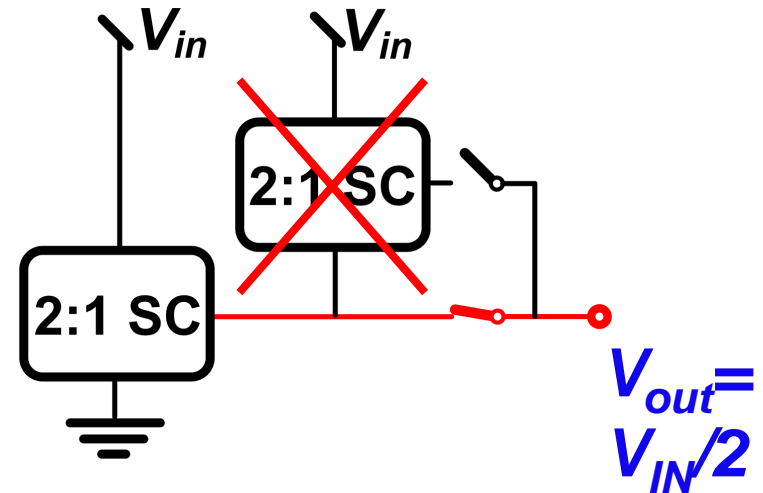
Cells Stacked for 3/4



Cells cascaded for 1/4



Route V_{out} from 1st cell for 1/2

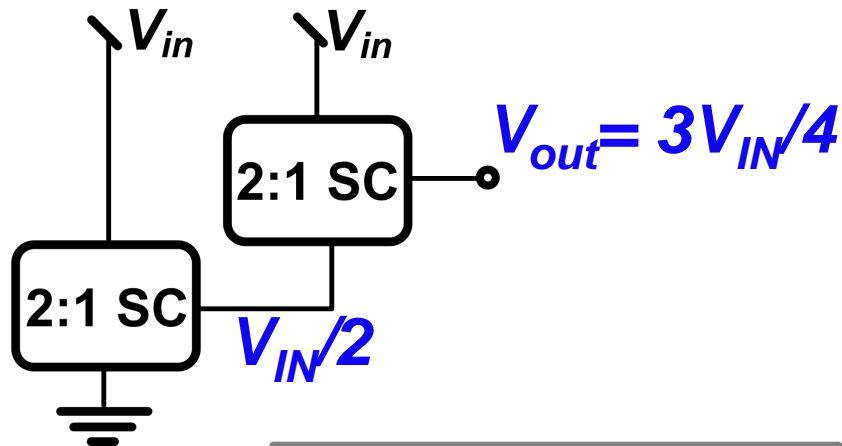


Wastes the capacitance of the 2nd cell, lower η

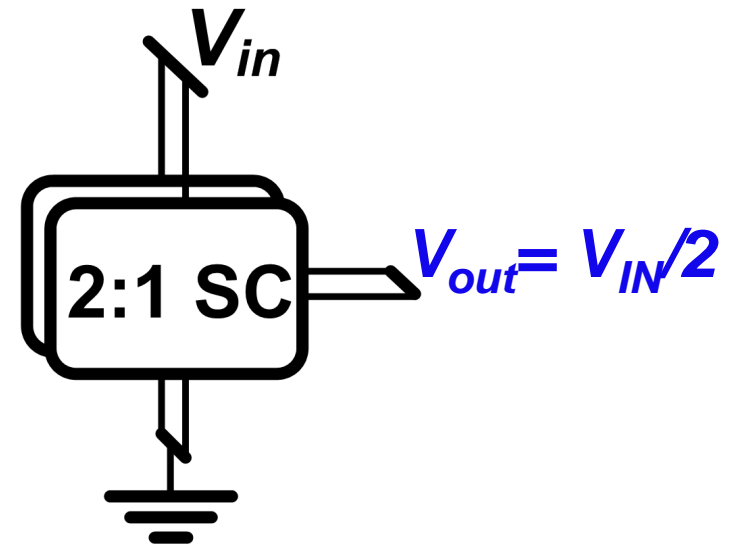
Recursive SC Ratio Reconfiguration

- 1/4, 3/4 are realized, how to get 1/2

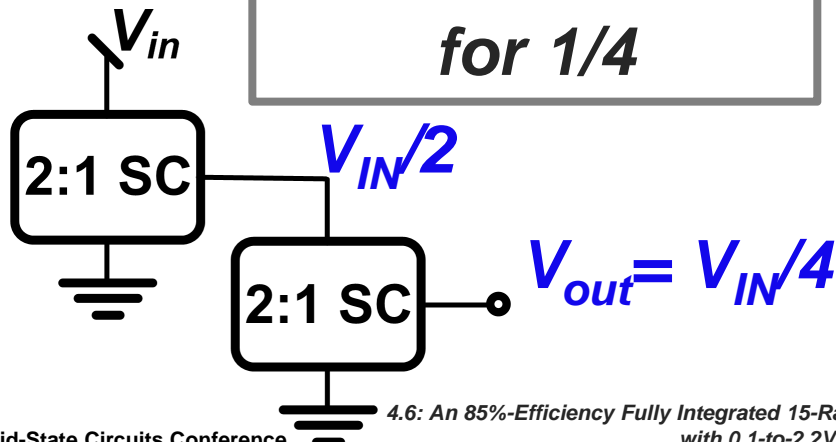
Cells Stacked for 3/4



Cells in parallel for 1/2



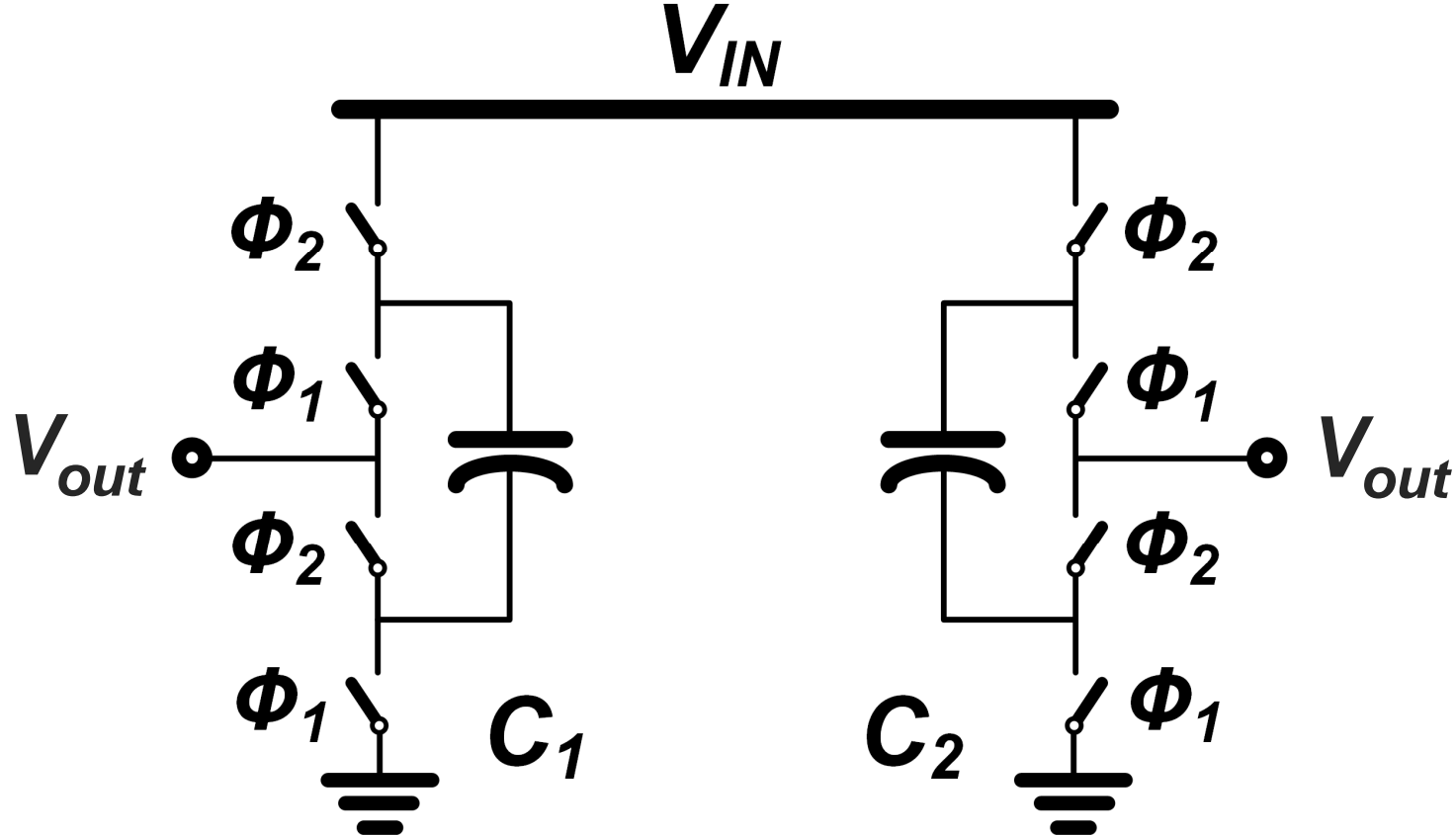
Cells cascaded for 1/4



Recursive Inter-cell Connection: 100% of the Caps used among all ratios

Recursive Inter-Cell Connection

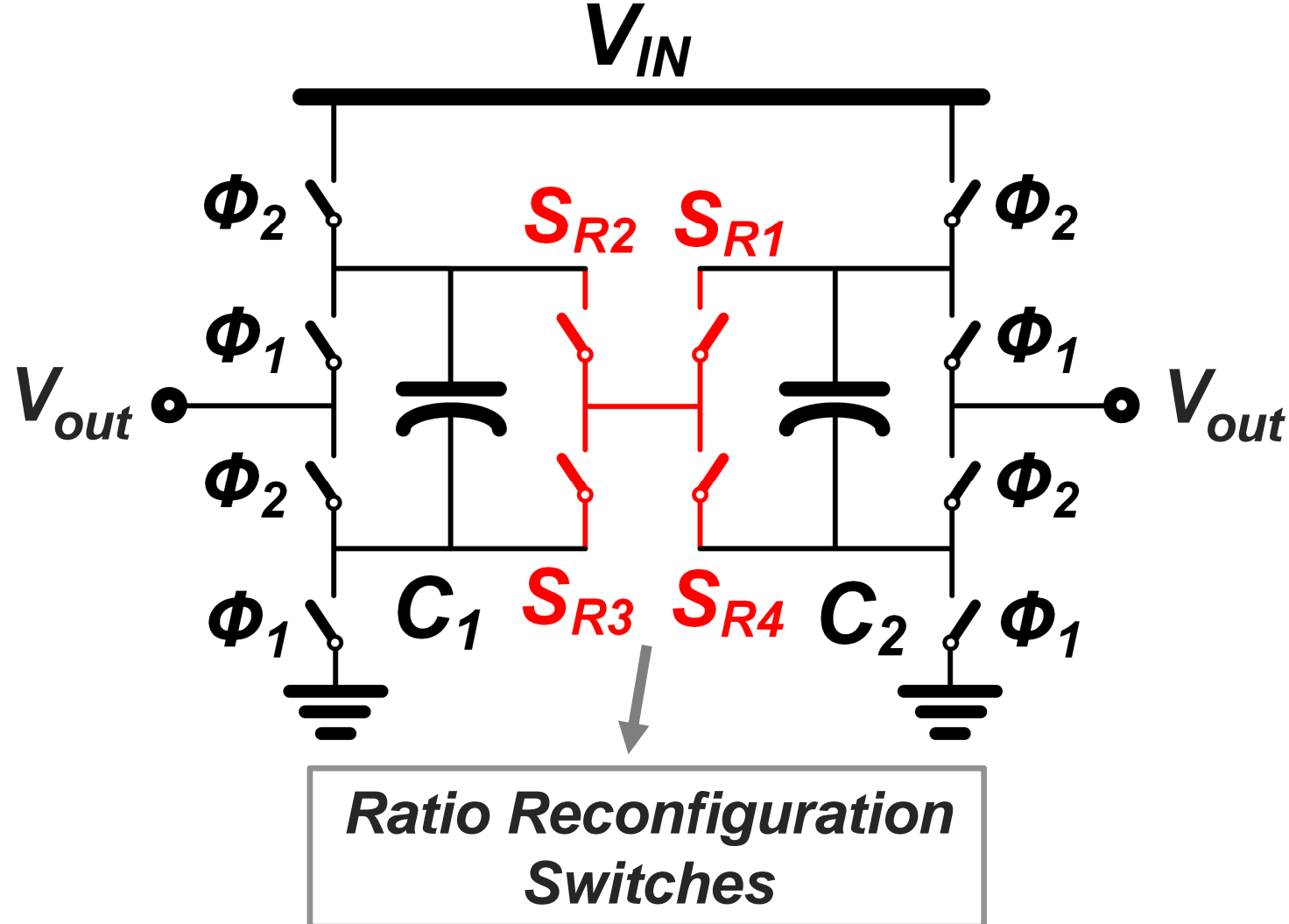
- How to realize $1/2$, the switch detail



Ratio = $1/2$
two cells in parallel

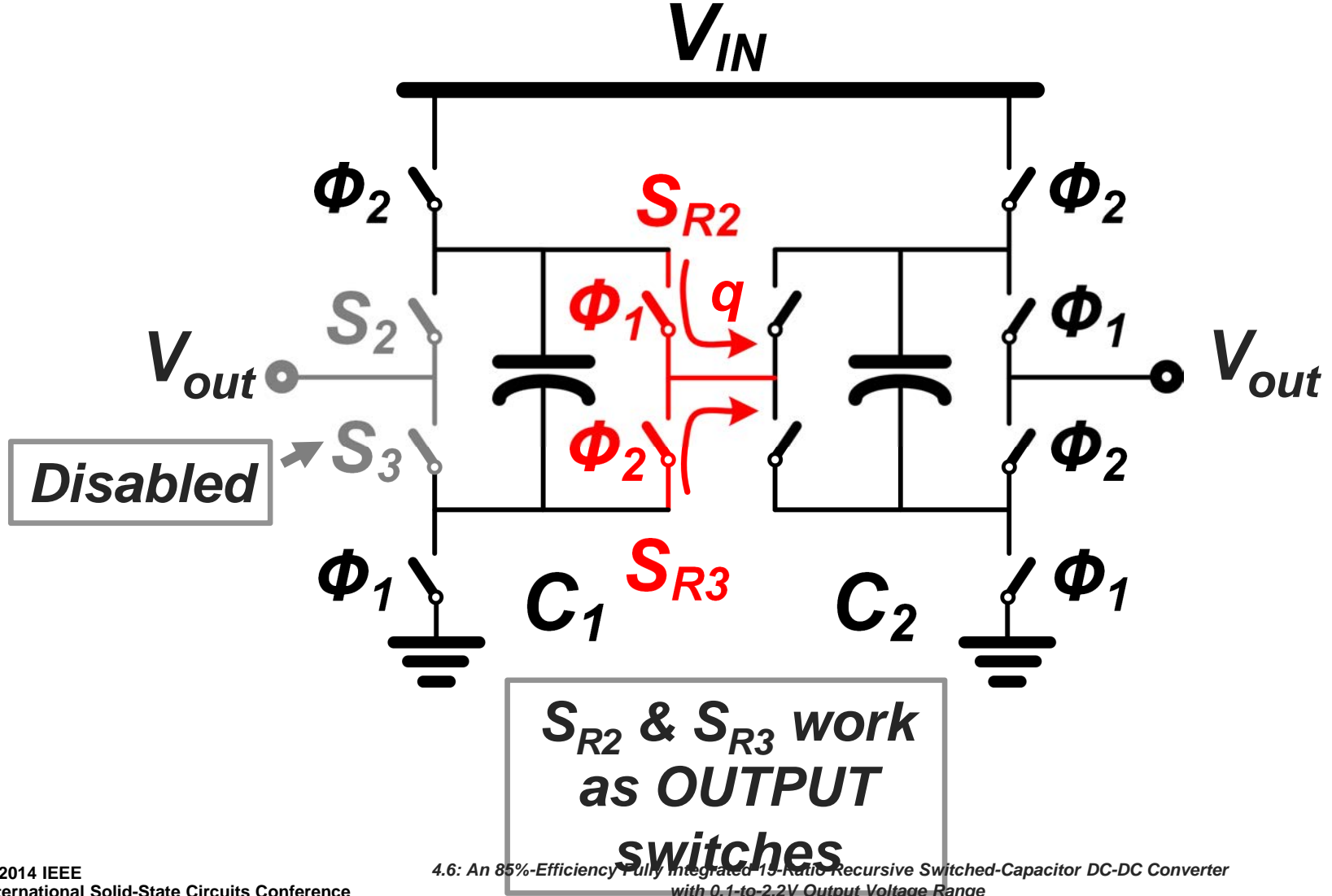
Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail



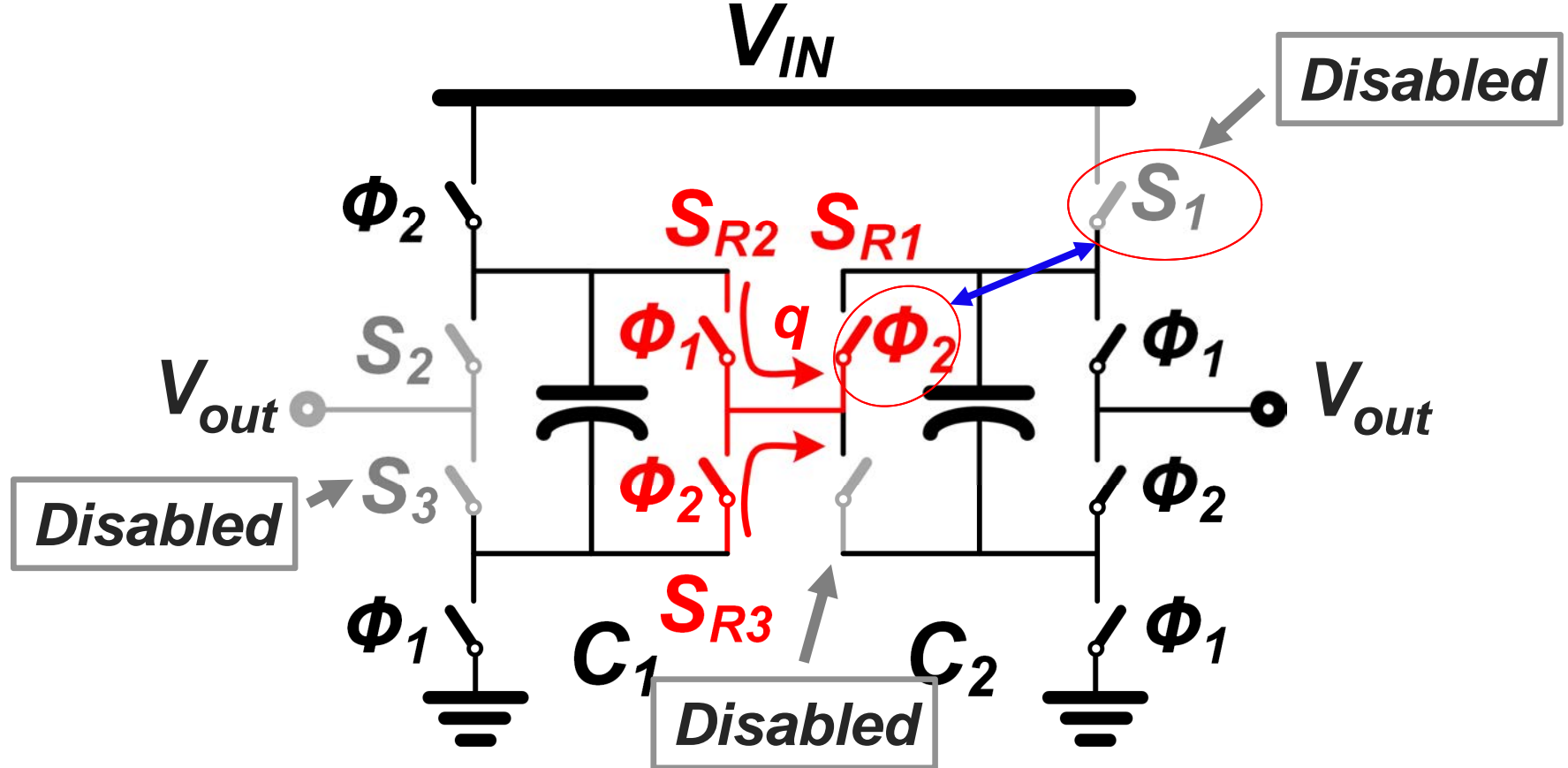
Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail



Recursive Inter-Cell Connection

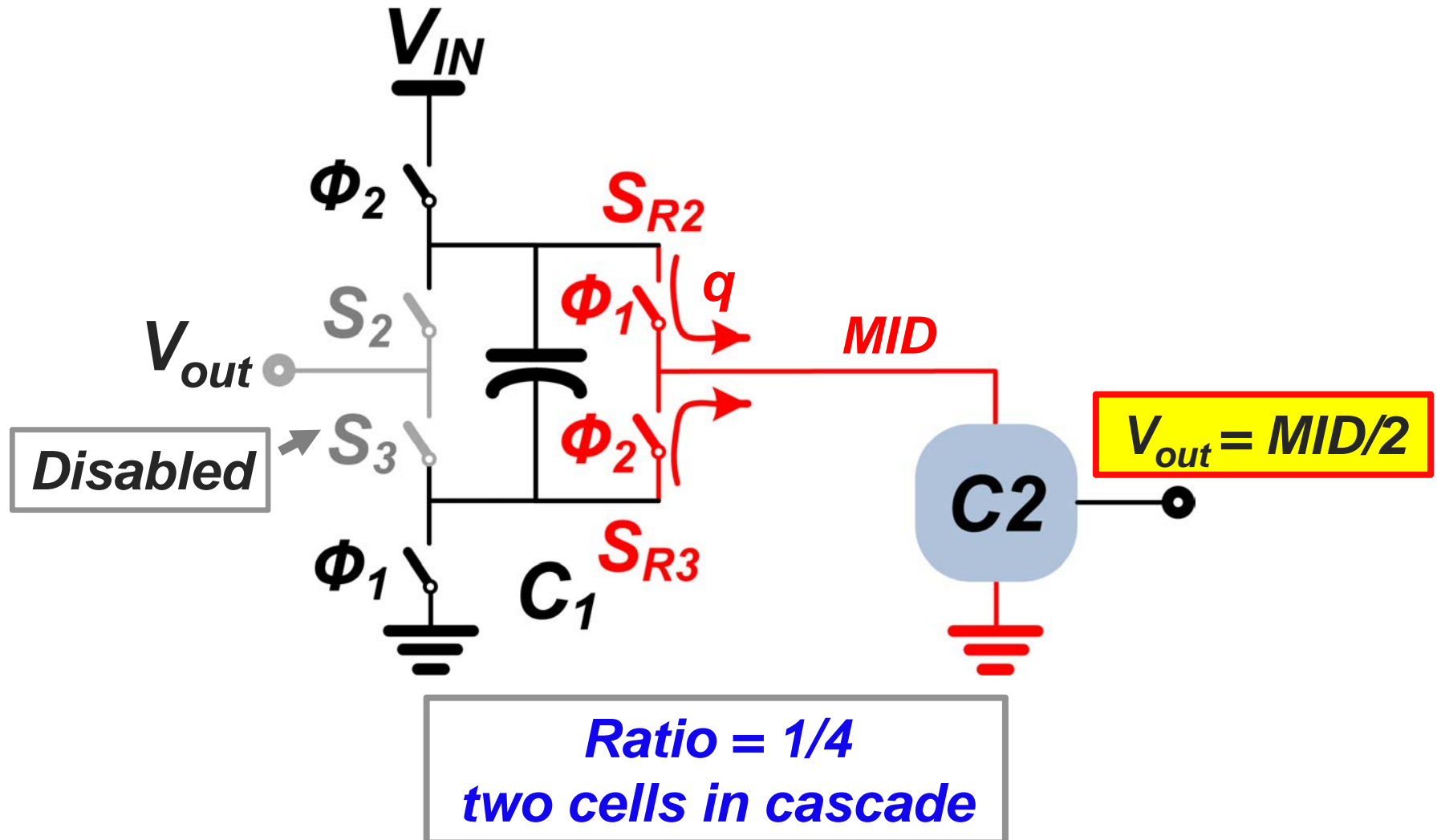
- How to realize 1/4, the switch detail



S_{R1} works as
INPUT switch S_1

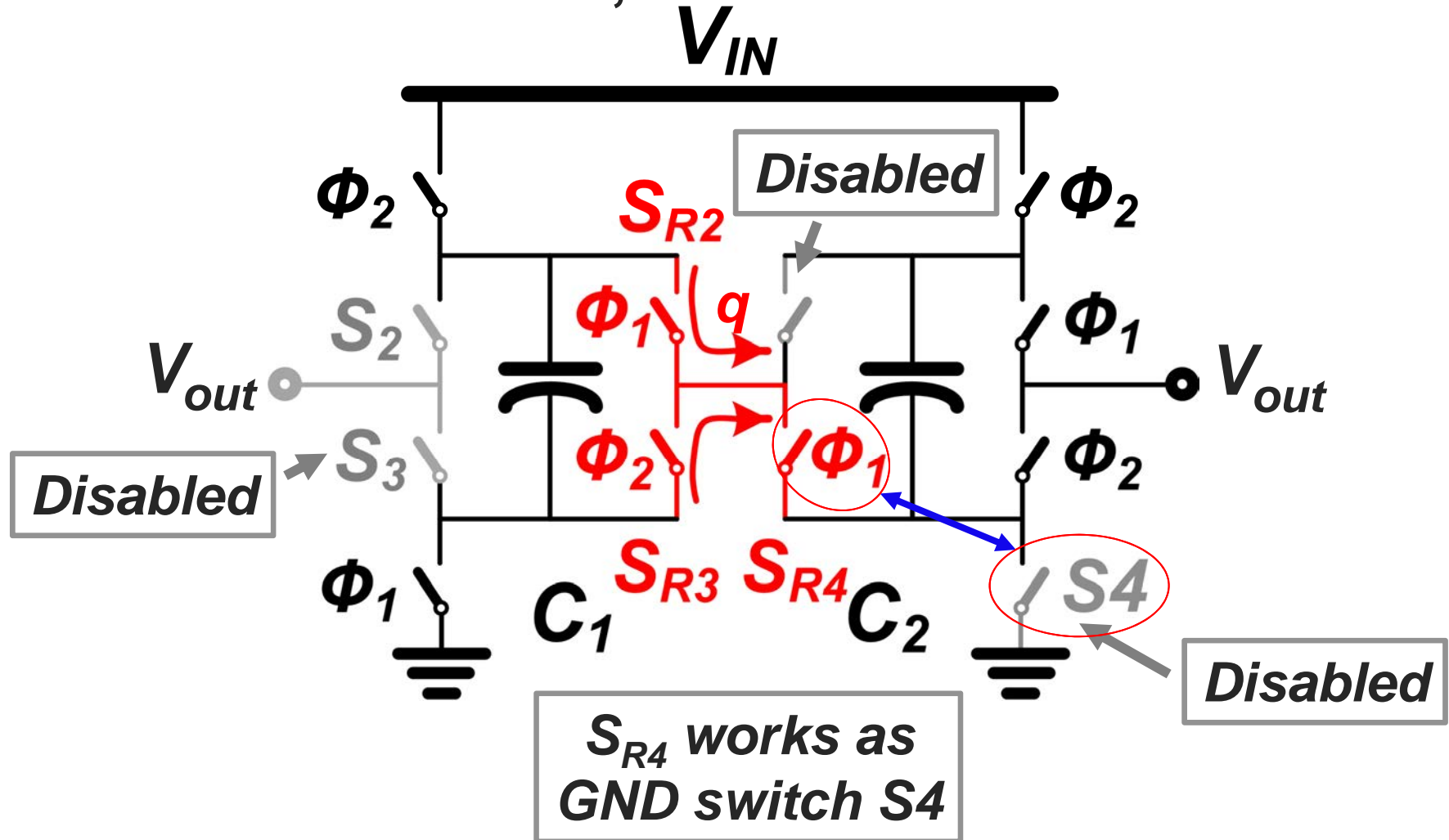
Recursive Inter-Cell Connection

- How to realize 1/4, the switch detail



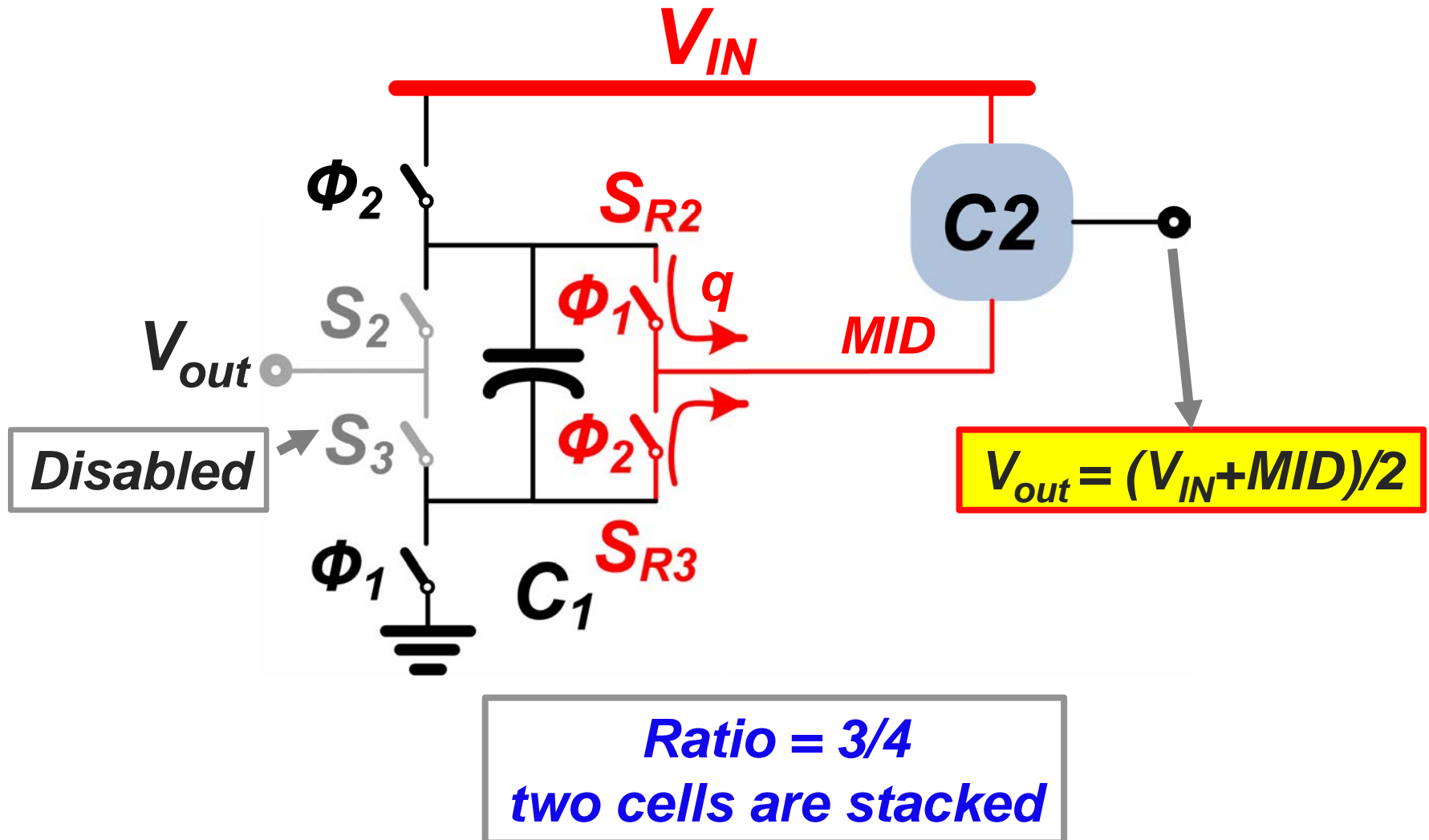
Recursive Inter-Cell Connection

- How to realize 3/4, the switch detail



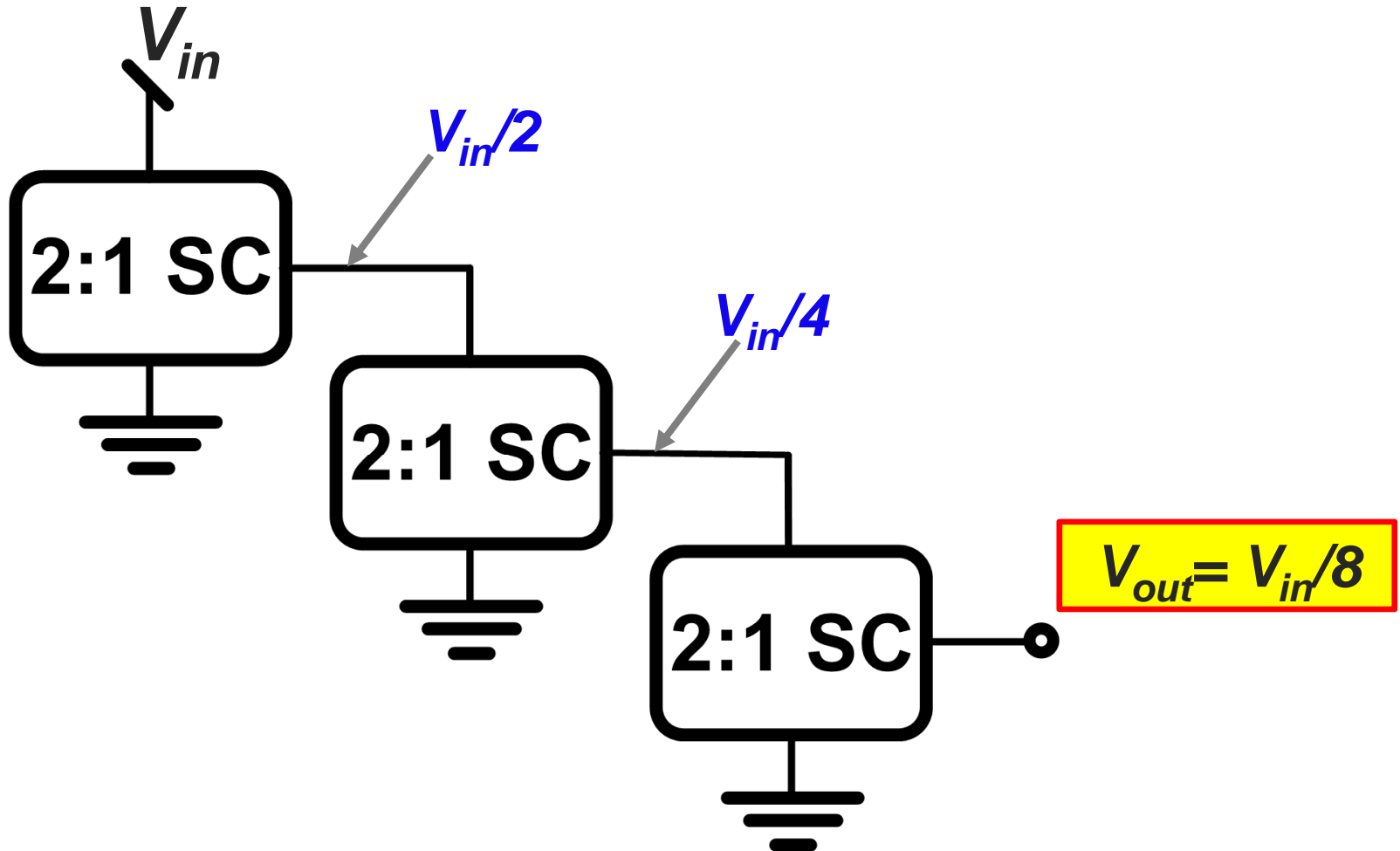
Recursive Inter-Cell Connection

- How to realize 3/4, the switch detail



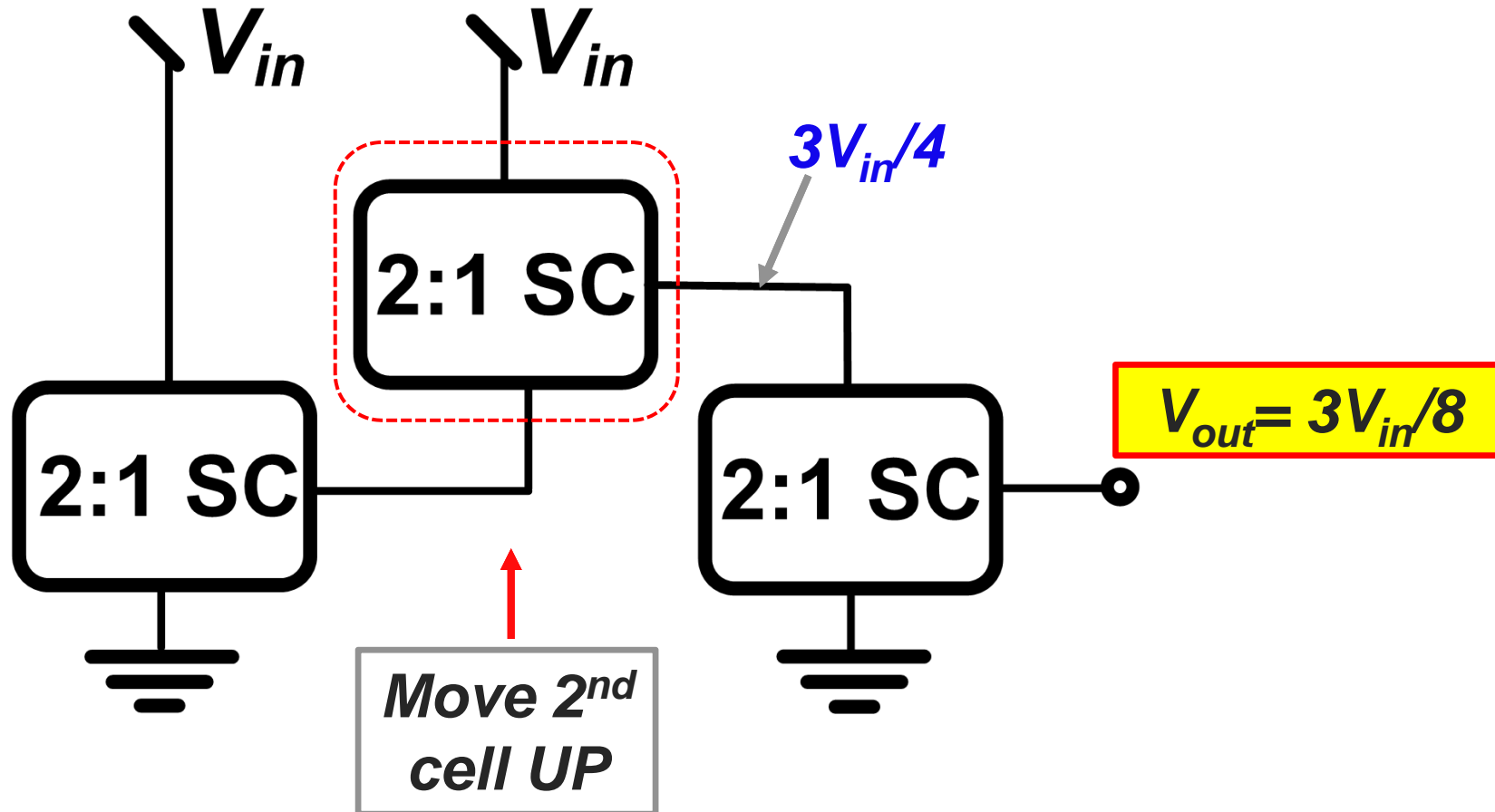
Recursive 3-bit SC

- Adding a third 2:1 SC cell: **resolution** = $V_{in}/2^3$



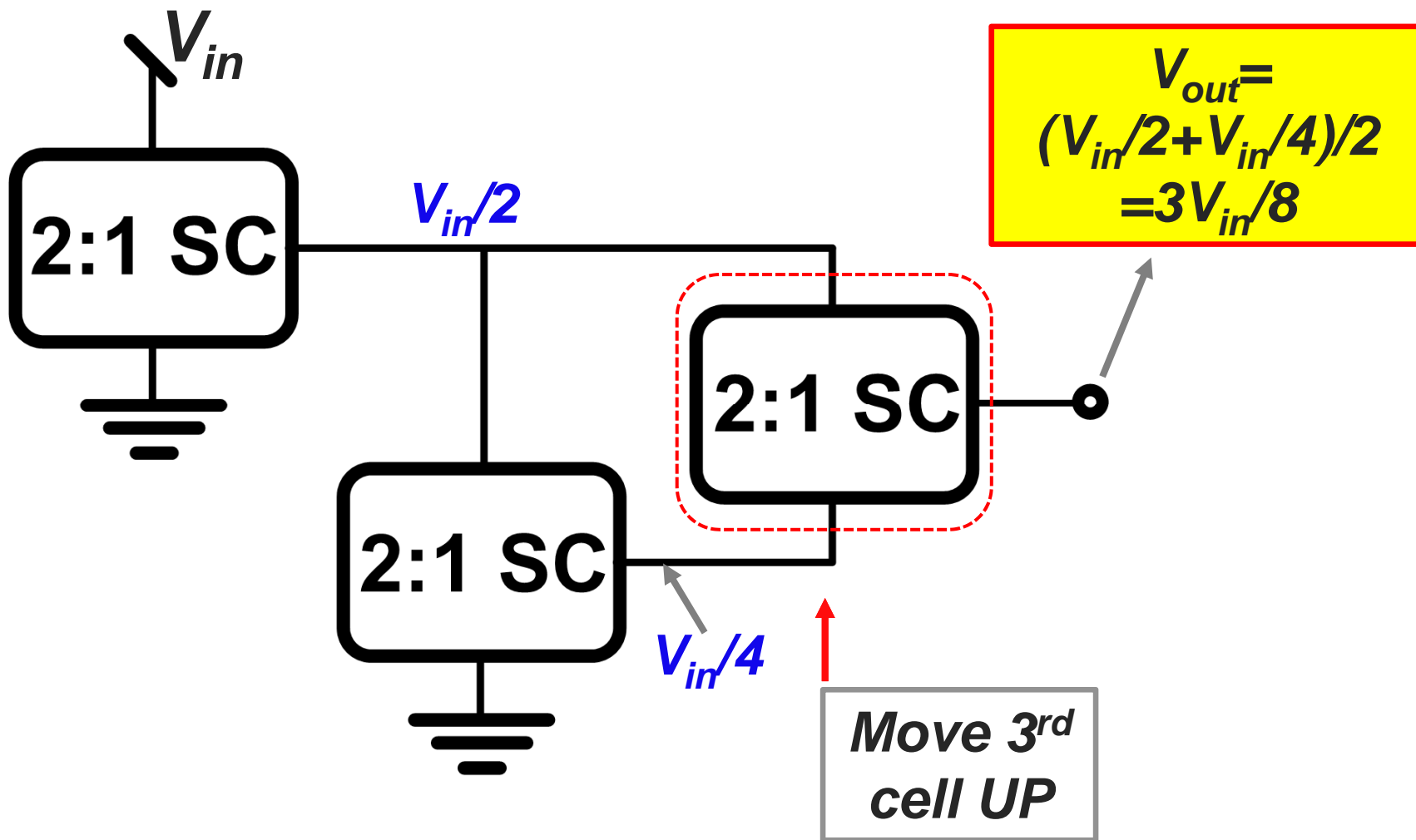
Recursive 3-bit SC

- Realizing 3/8 ratio



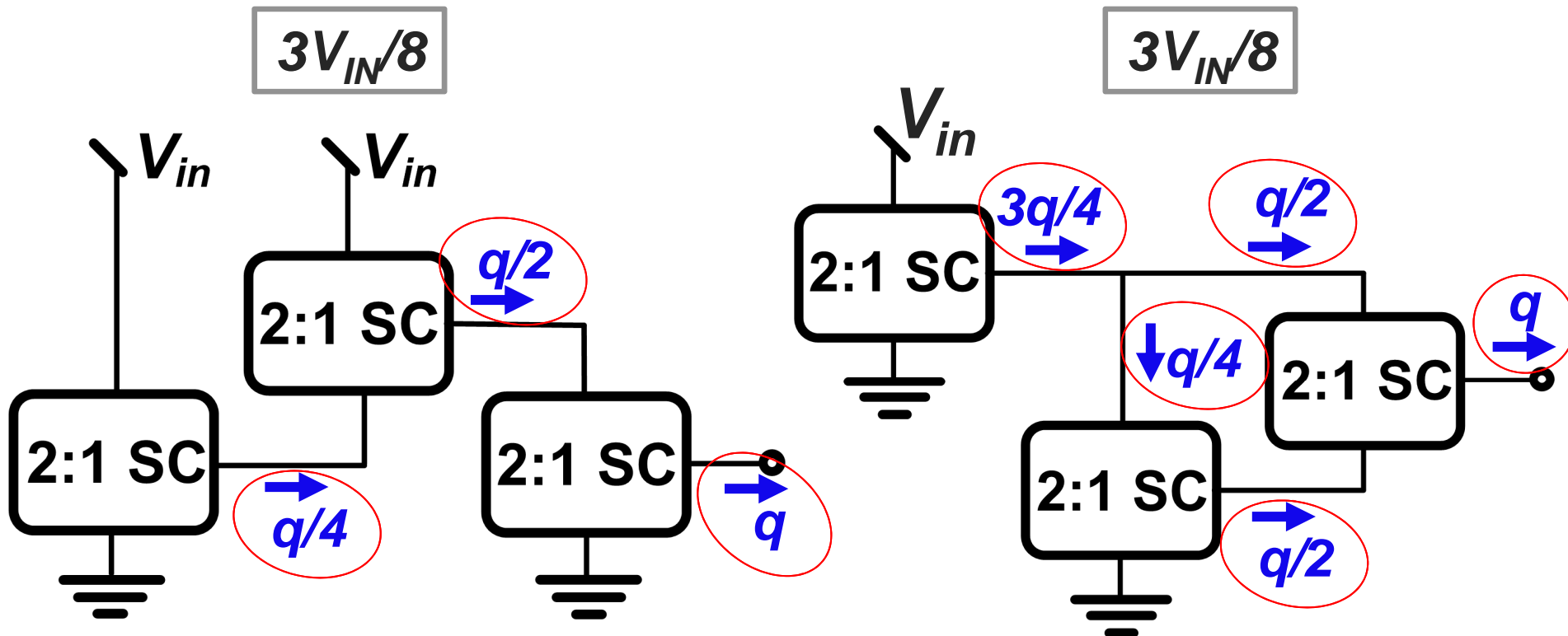
Recursive 3-bit SC

- Another way to realize 3/8 ratio



Recursive 3-bit SC

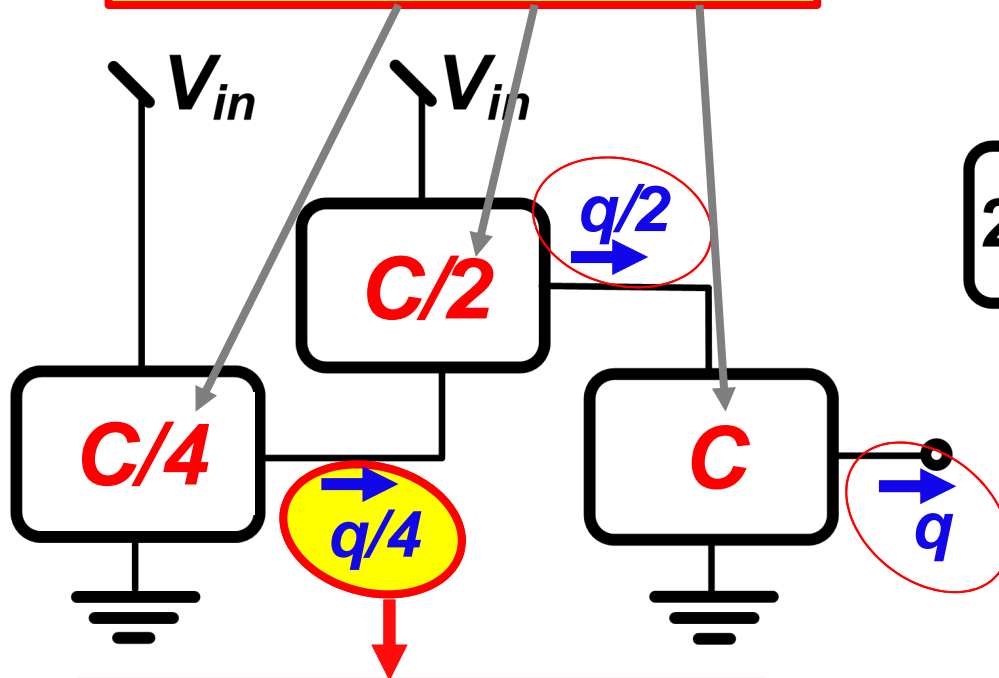
- Which one is better to realize $3/8$ ratio?



Recursive 3-bit SC

- Which one is better to realize 3/8 ratio?

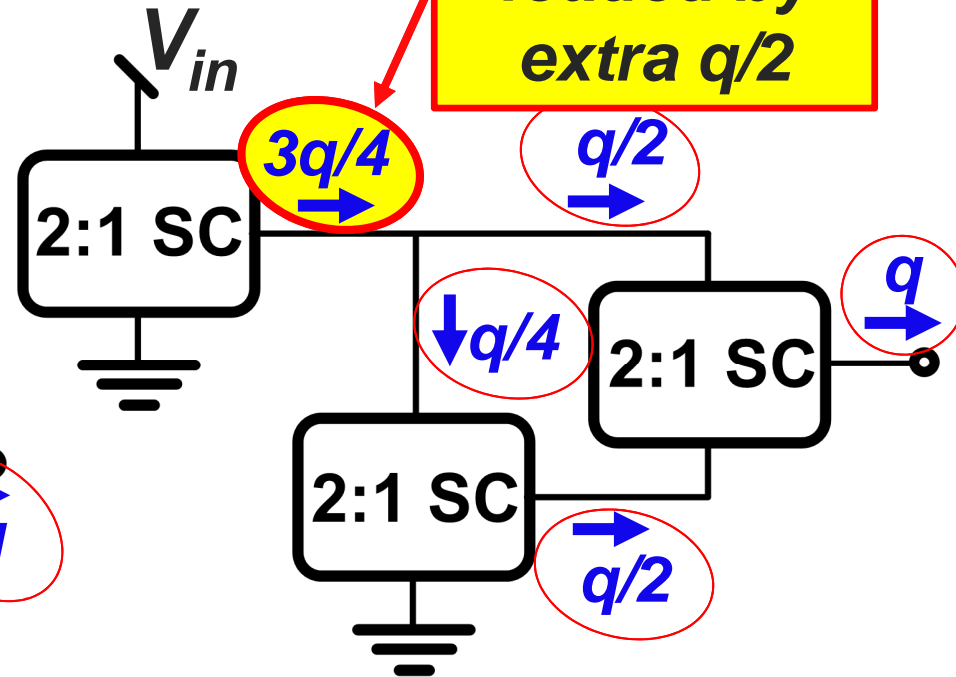
Binary relative sizing



For same q output, SC is less loaded, thus lower losses

Higher η

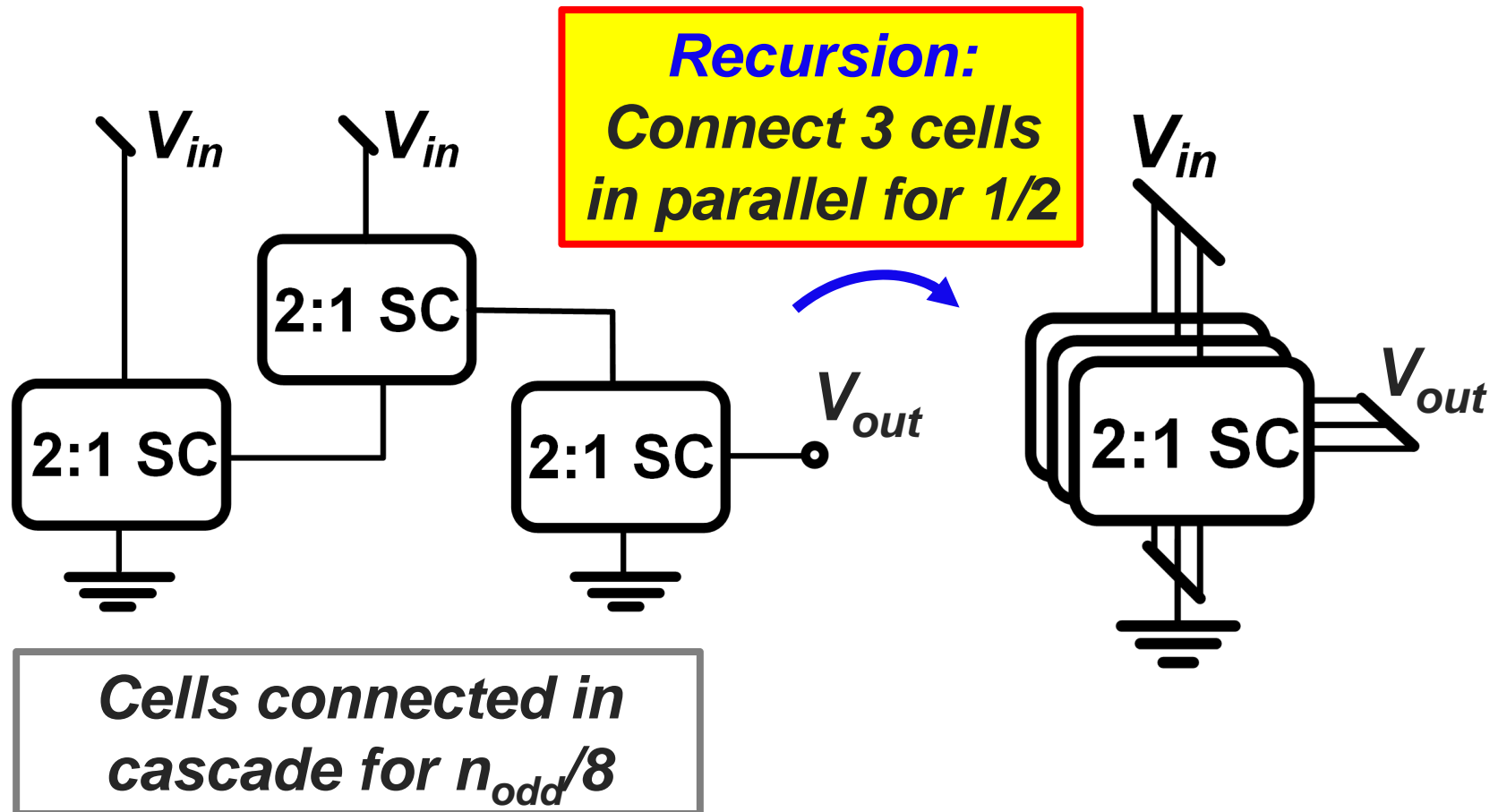
1st Cell is loaded by extra $q/2$



Maximizing V_{in} & GND connections maximizes η

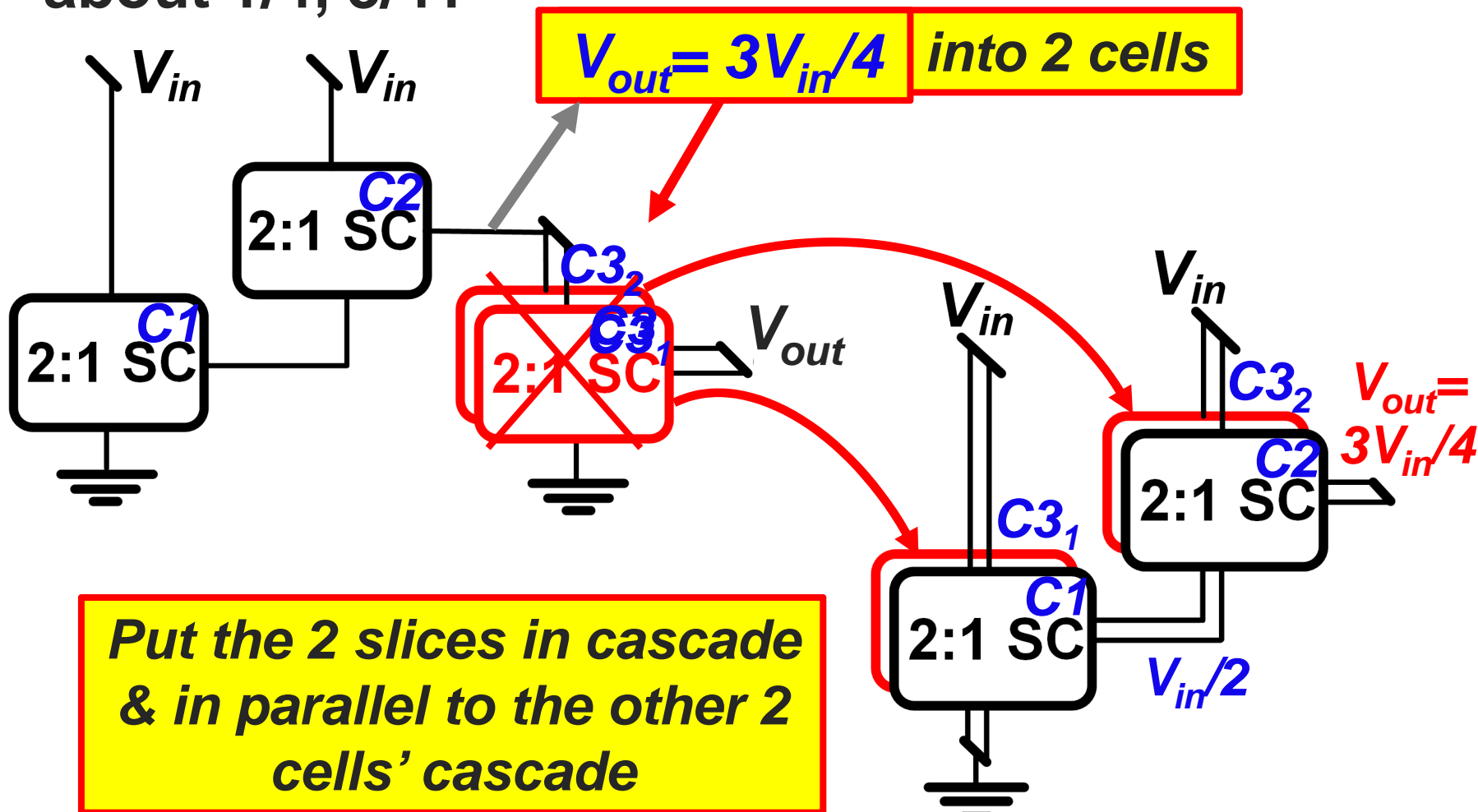
Recursive 3-bit SC: 1/2 Realization

- Now $1/8$, $3/8$, $5/8$, $7/8$ are realized, how to achieve $1/2$ using 3 cells?



Recursive 3-bit SC: 1/4, 3/4 Realization

- Now 1/8, 3/8, 5/8, 7/8, and 1/2 are realized, what about 1/4, 3/4?



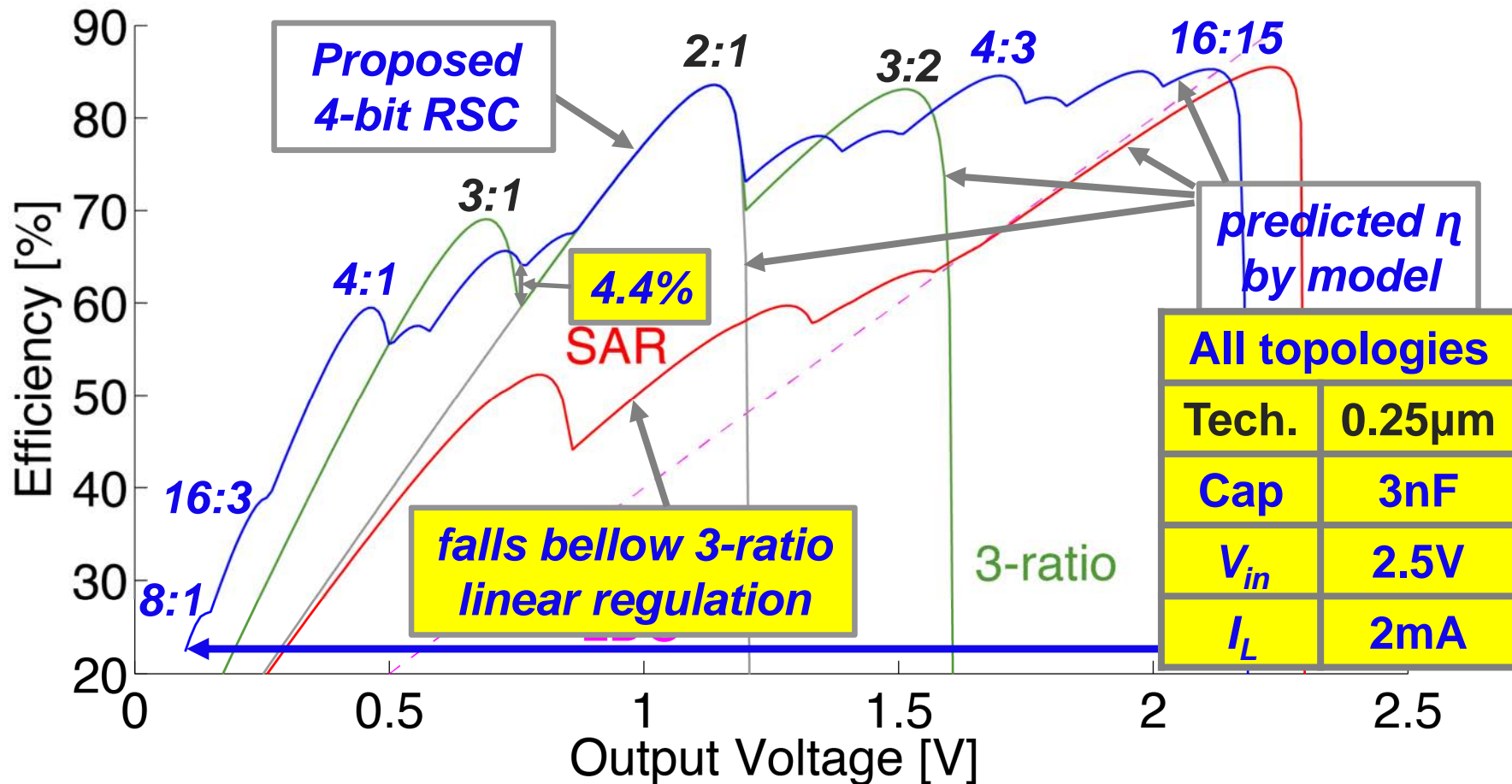
Recursive 4-bit SC

- A **4-bit Recursive SC** topology is implemented
 - *Balance between complexity and flat η*

Realizing 15-ratio, of high η by:

- ***Recursive inter-cell connection for 100% cap utilization***
- ***Maximizing V_{in} & GND connections***
- ***Binary relative sizing***

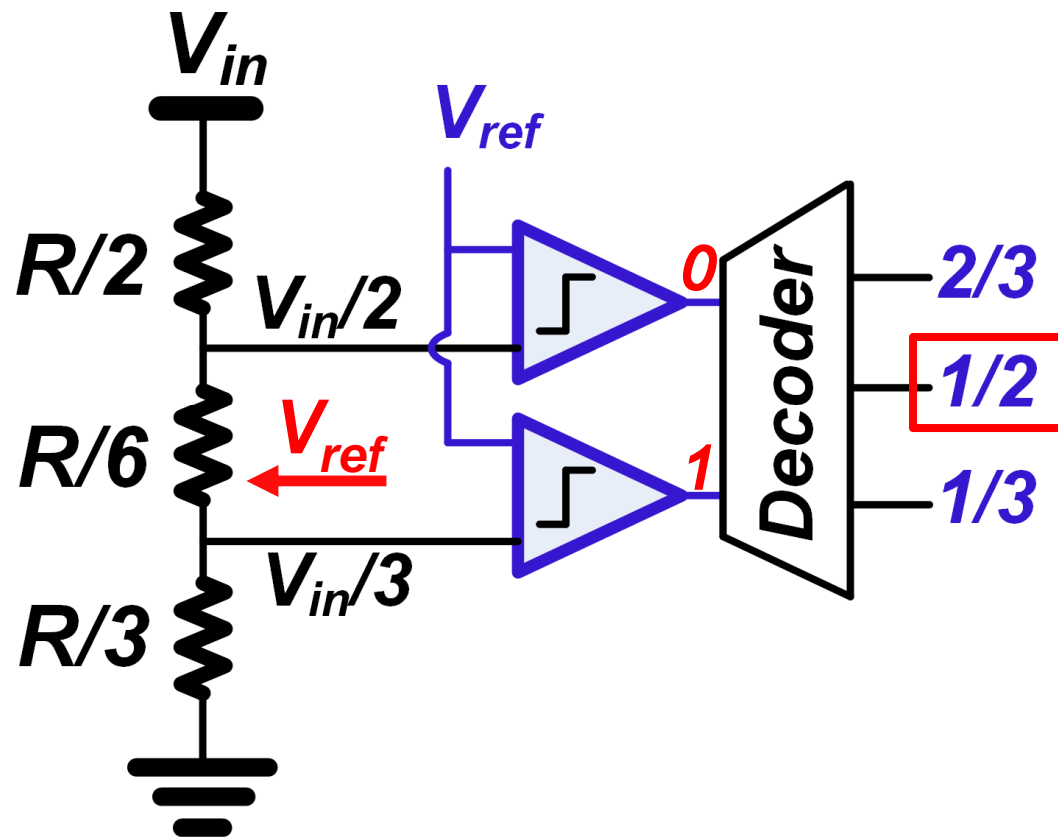
4-bit Recursive SC Efficiency vs. V_{out}



For same silicon area: widest operating range, highest average efficiency

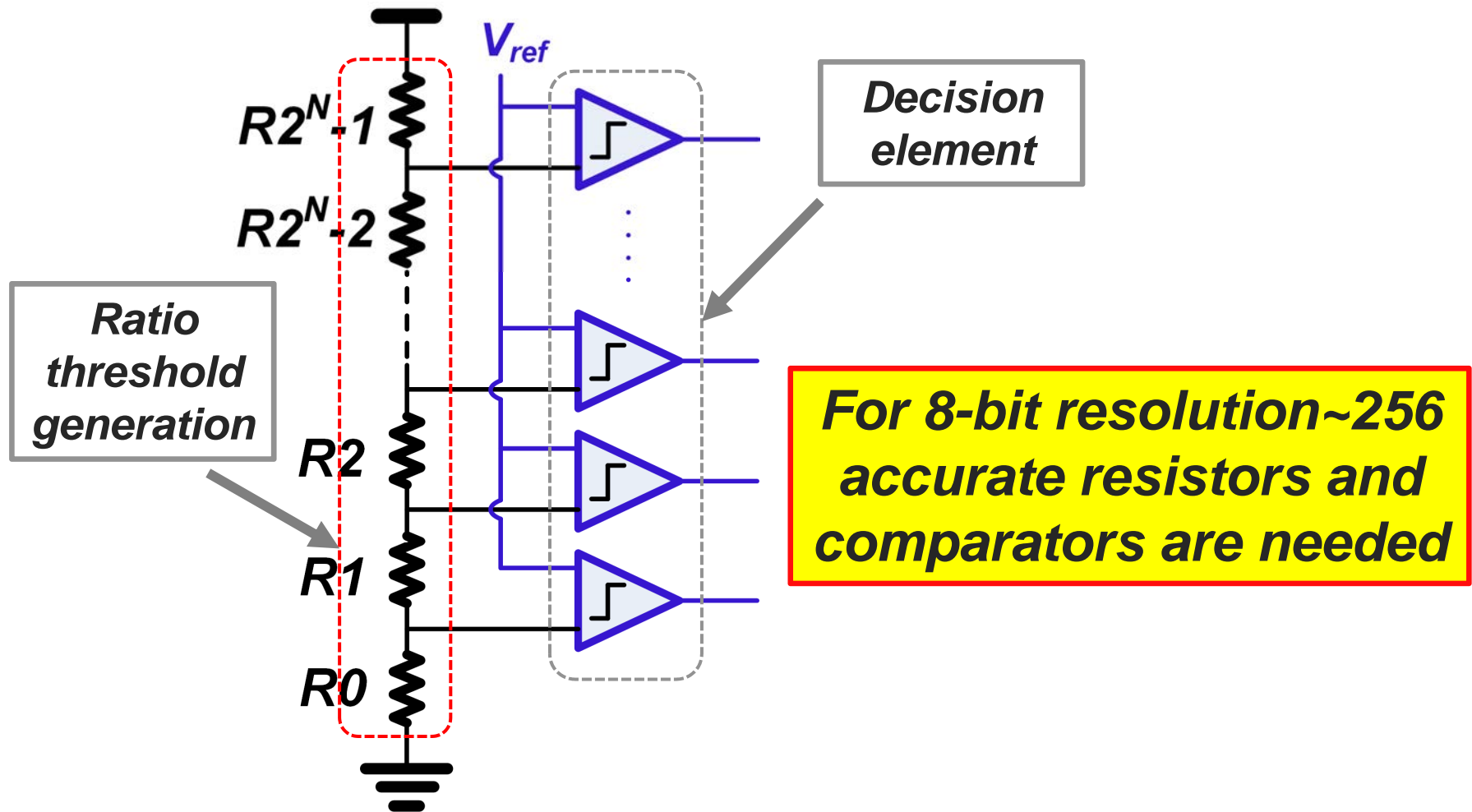
Typical Multi-Mode SC Control

- Compare V_{ref} (desired output) with levels from a resistor string to find desired ratio



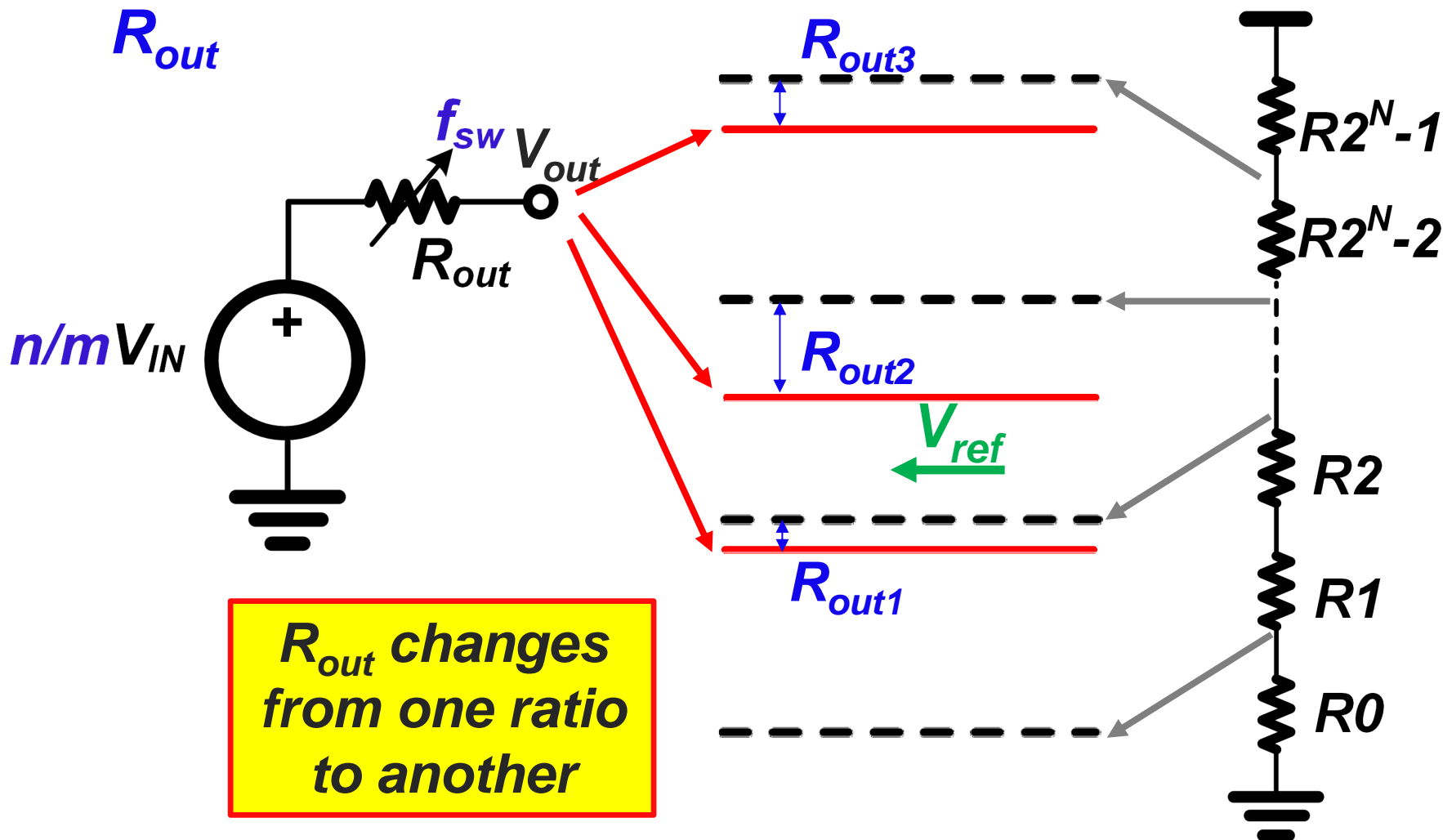
Typical Multi-Mode SC Control

- Challenge of large number of ratios



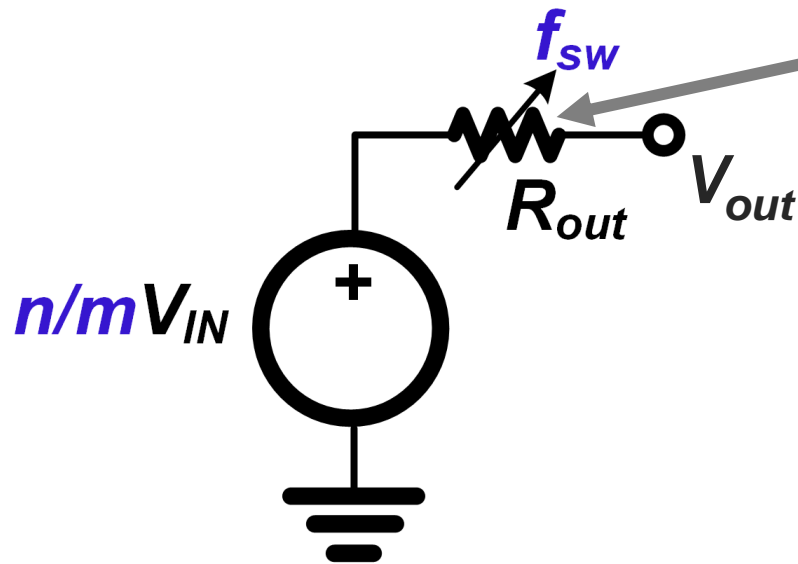
Typical Multi-Mode SC Control

- Ratios' threshold levels mismatch due to SC



All-Digital Binary Search Control

- **Solution: Ratios' threshold levels are produced by the SC itself**

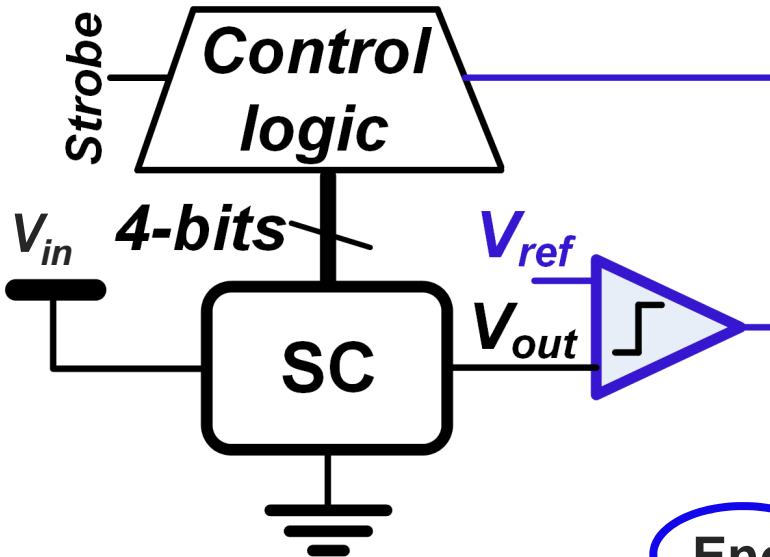


Switching at highest f_{sw} , R_{out} is min

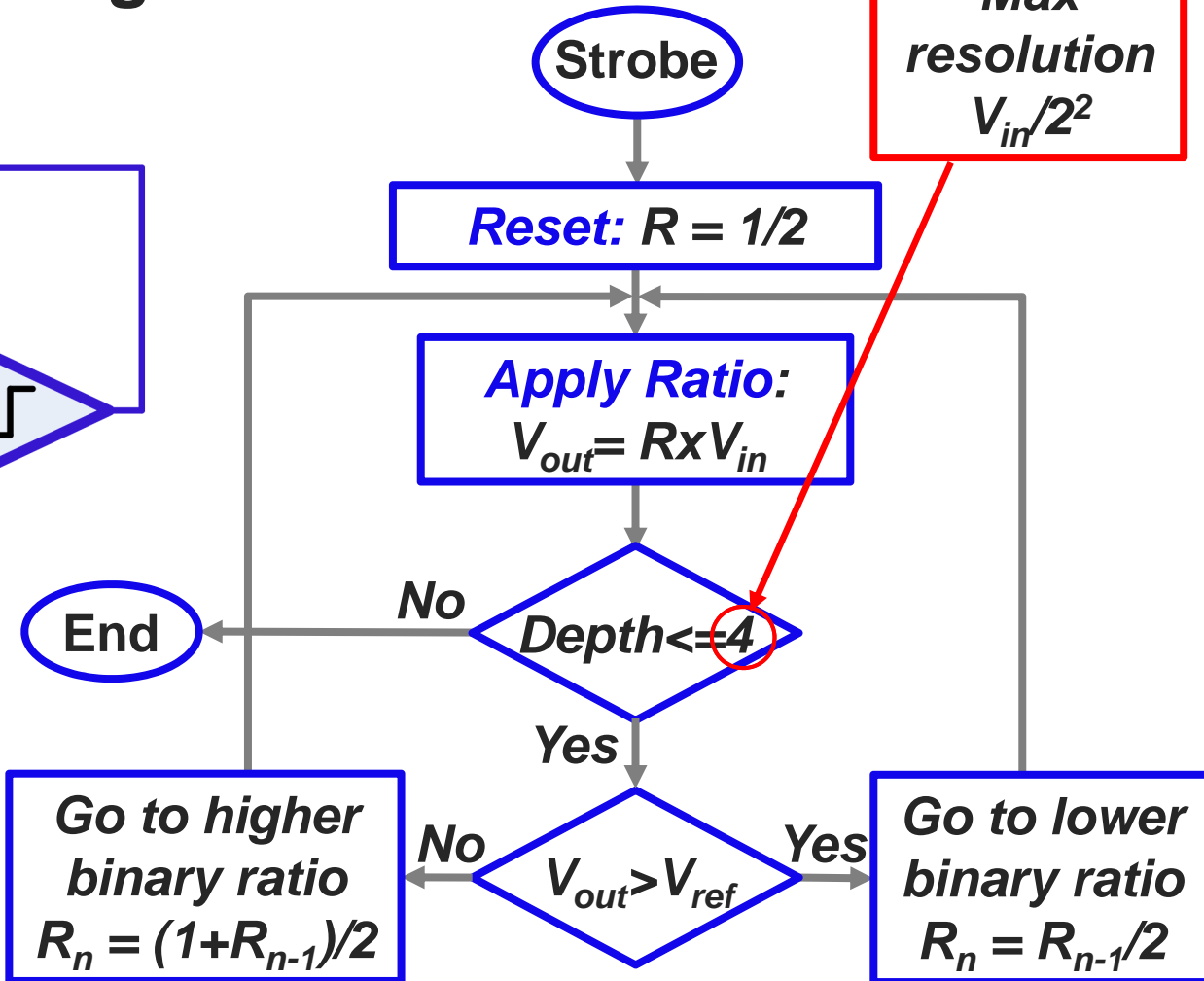
SC outputs the max V_{out} for certain n/m RATIO

All-Digital Binary Search Control

- Binary Search Algorithm:

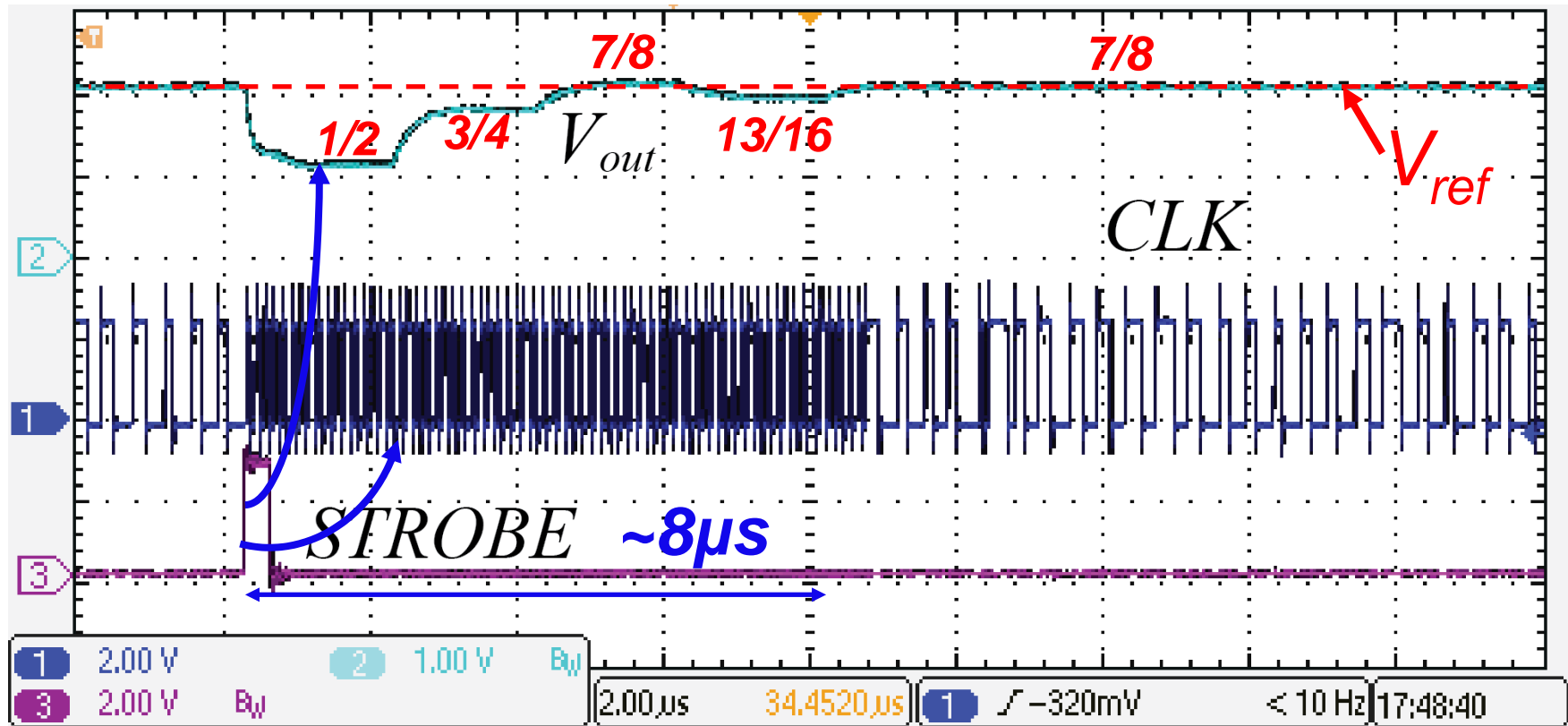


- No resistor string
- 1 comparator & simple gates
- No R_{out} mismatch

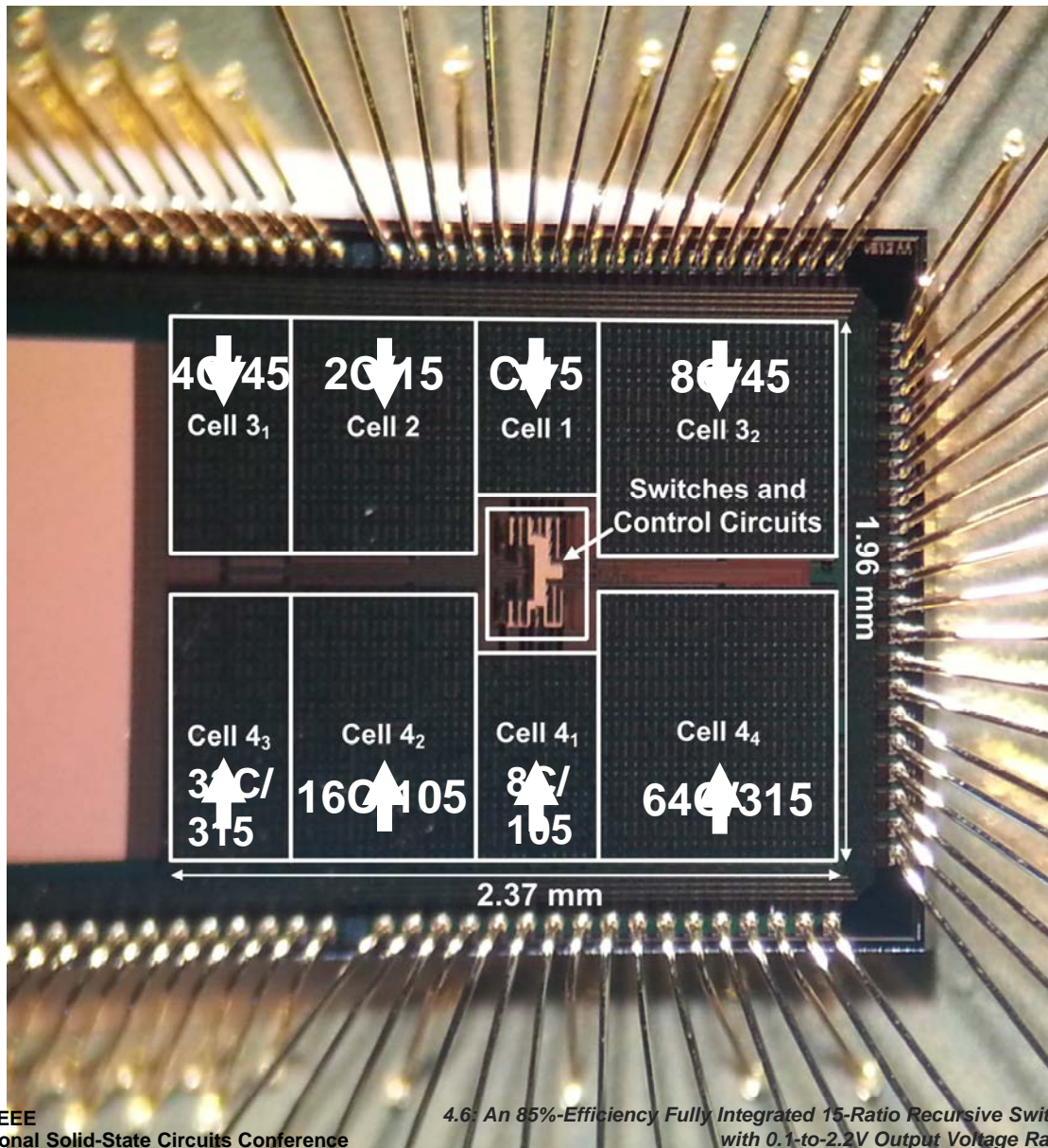


Measured Controller Transient Response

- 8 μs response time



Fully Integrated Recursive 4-bit SC Prototype



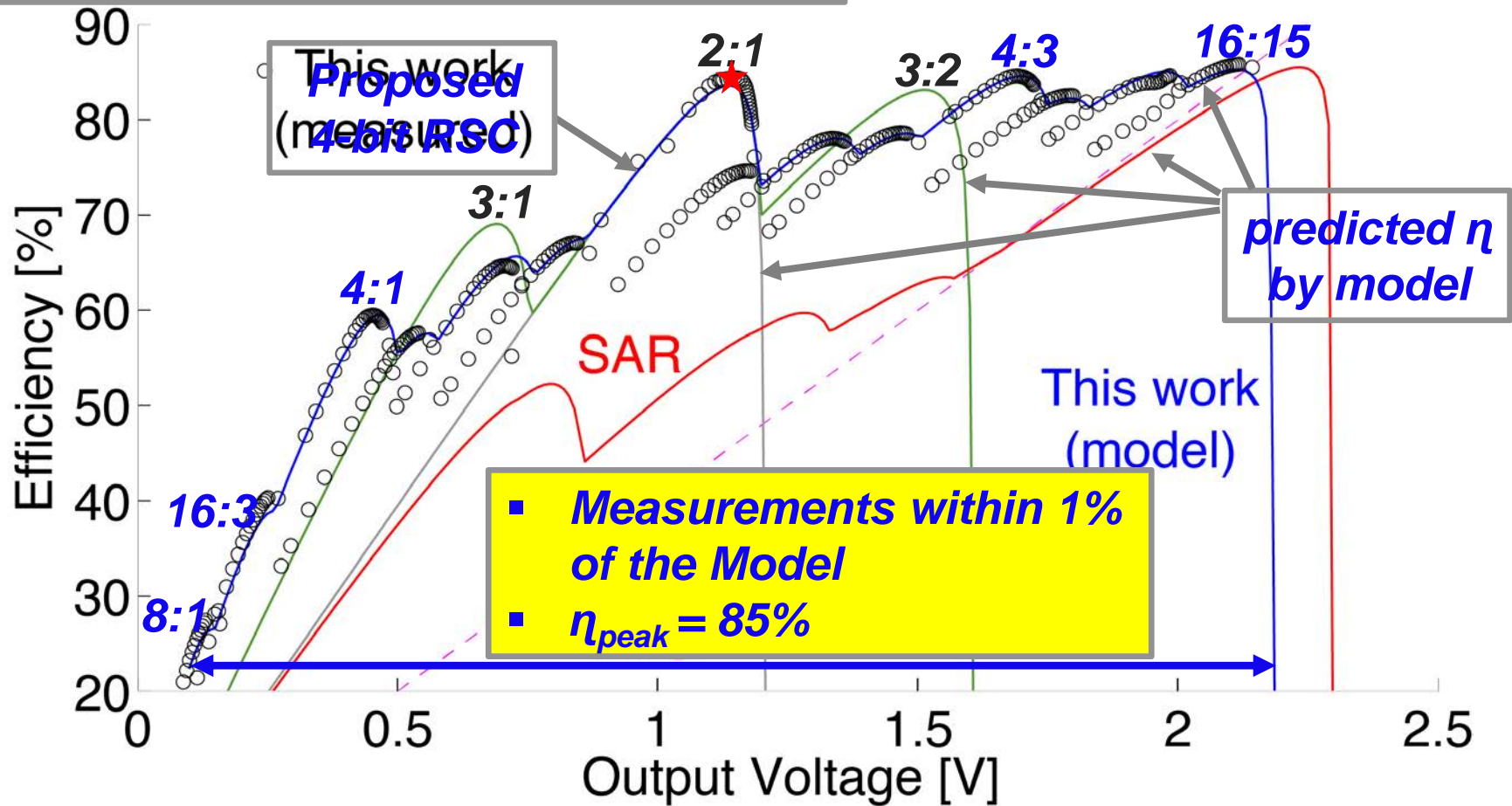
*0.25μm 2.5V
bulk CMOS
MIM ~ 0.9 fF/μm²*

➤ 8 2:1 cells are used to enable recursion

➤ Cells are binary weighted for optimal relative sizing

Measured Efficiency vs. V_{out}

0.25 μ m: Cap = 3nF, V_{in} = 2.5, I_L = 2mA

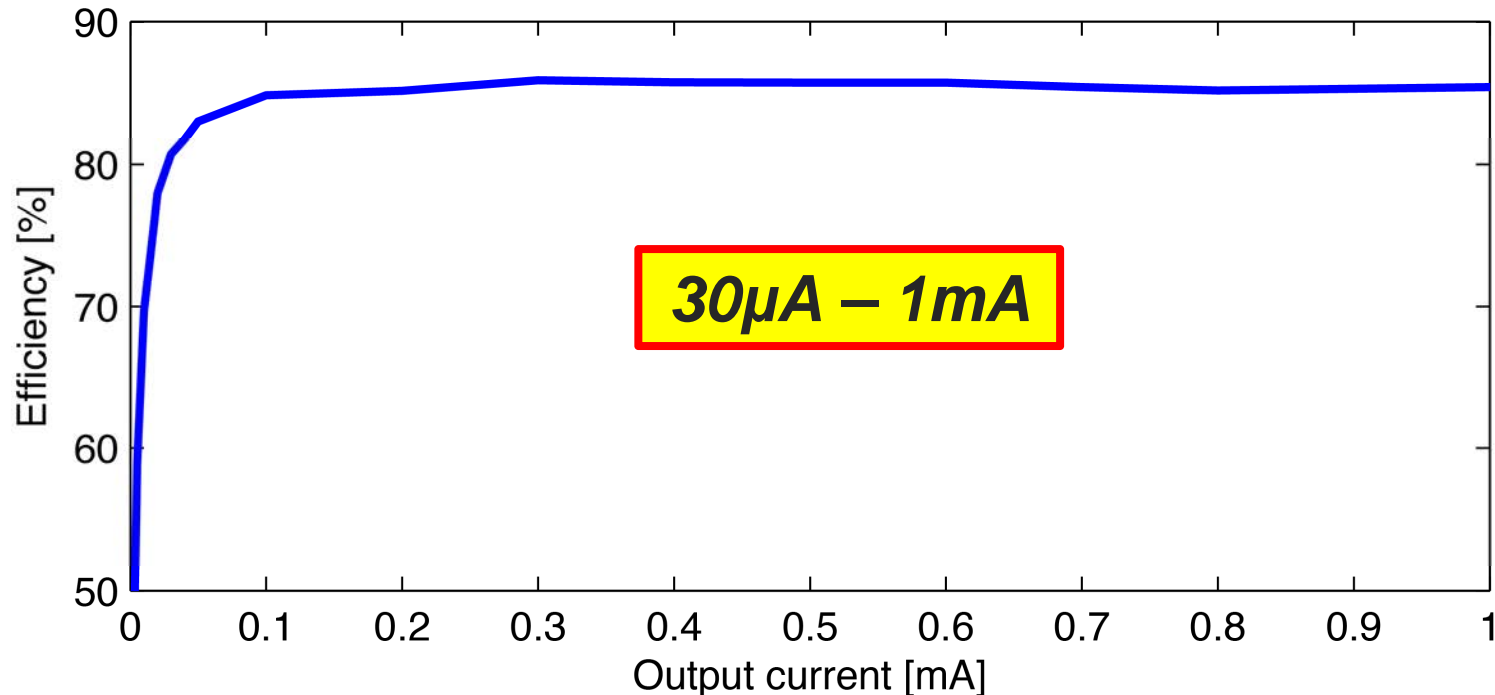


For same silicon area: widest operating range, highest average efficiency

4.6: An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter with 0.1-to-2.2V Output Voltage Range

Measured Efficiency vs. I_L

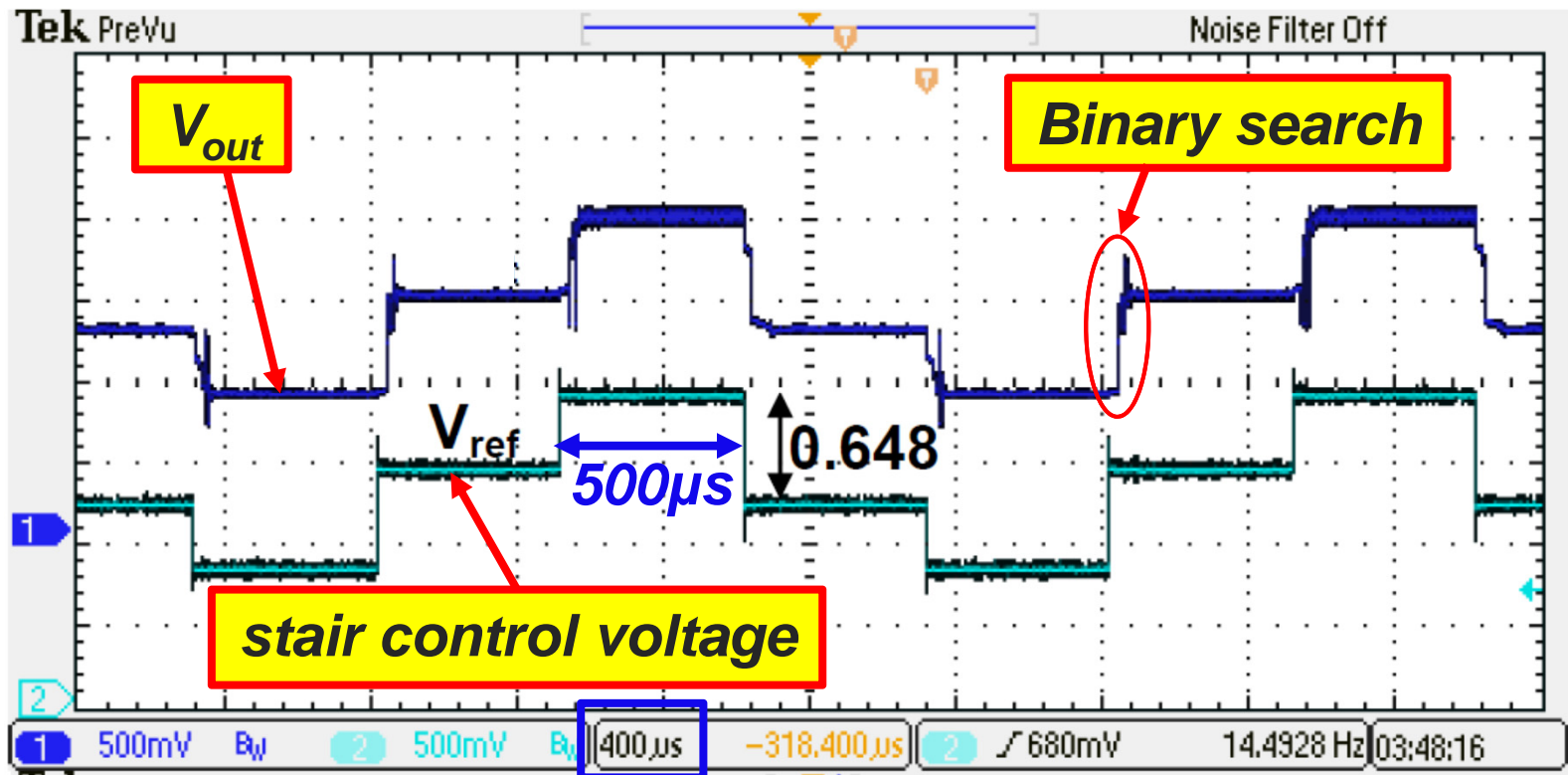
0.25 μm : $C = 3\text{nF}$, $V_{in} = 2.5$, Ratio = 1/2



**Switching losses scale
with lower power levels**

Measured Controller Transient Response

- Tracking an input stair control voltage



Conclusions

- A new Modular SC topology comprising individual 2:1 SC
- High η through:
 - *Recursive interconnection* achieving 100% cap utilization
 - *Maximizing V_{in} & GND connections* for minimum overhead charge through the SC
 - *Optimal resource allocation (C,G) through BINARY* relative sizing

Highest average η & widest operating range amongst other SC topologies for same silicon area

A Sub-ns Response On-chip Switched-Capacitor DC-DC Voltage Regulator Delivering $3.7\text{W}/\text{mm}^2$ at 90% Efficiency Using Deep-Trench Capacitors in 32nm SOI CMOS

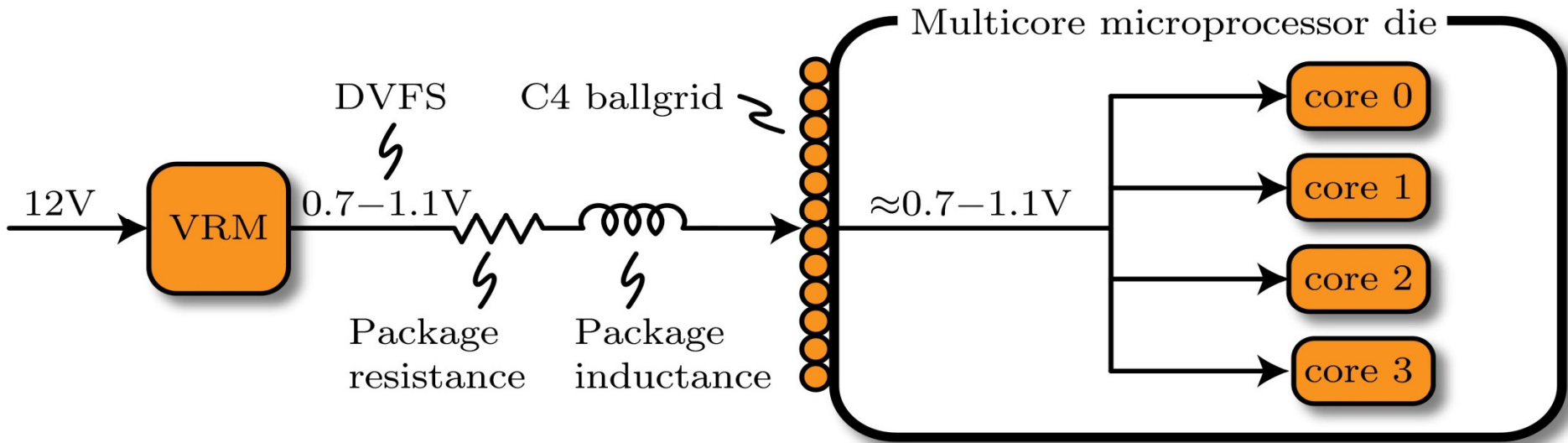
Toke Meyer Andersen^{1,2}, Florian Krismer¹, Johann W. Kolar¹, Thomas Toifl², Christian Menolfi², Lukas Kull², Thomas Morf², Marcel Kossel², Matthias Brändli², Peter Buchmann², Pier Andrea Francesc²

¹Power Electronic Systems Laboratory, ETH Zurich, Switzerland

²IBM Research Zurich, Rüschlikon, Switzerland

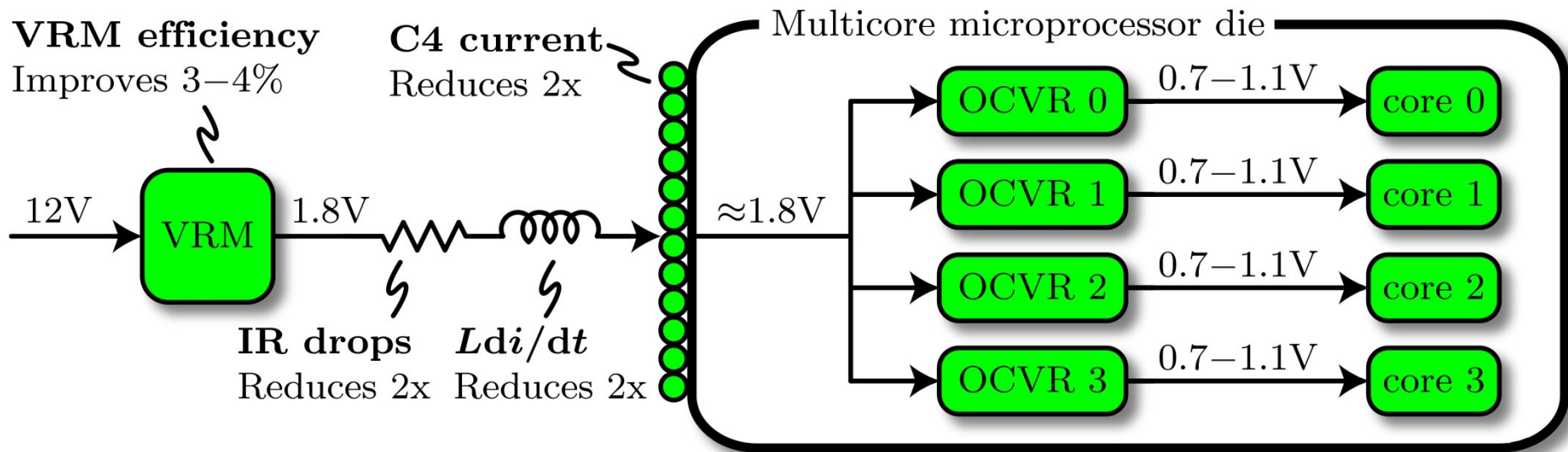


Microprocessor power delivery – Today



Microprocessor power delivery – Target

On-Chip Voltage Regulator (OCVR)



OCVR requirements:

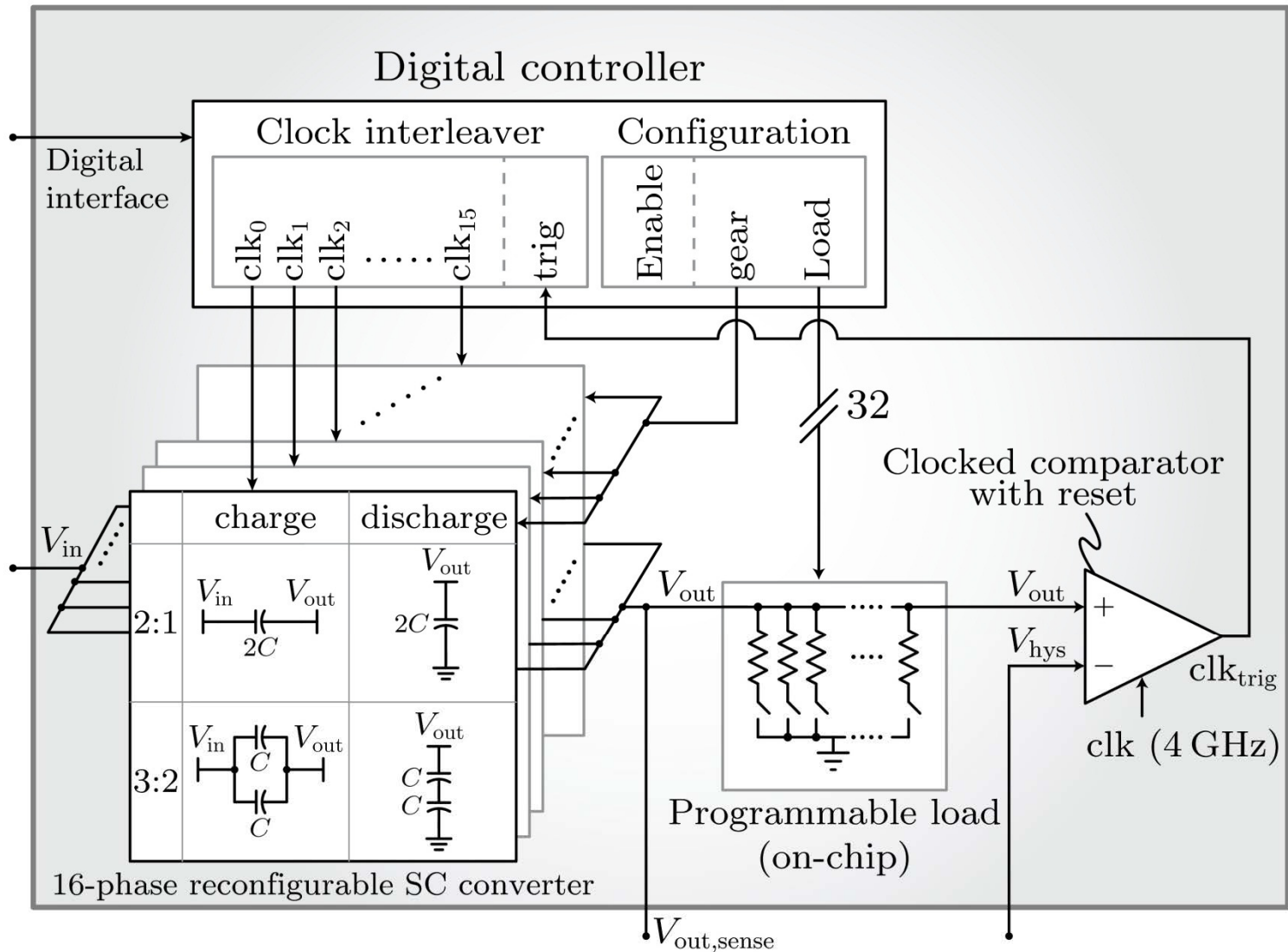
- >75%
- >1W/mm²
- <10ns
- >0.5W

Voltage granularity

Improves efficiency up to 21%
(workload dependent [1])

[1] Wonyoung Kim et al., HPCA 2008

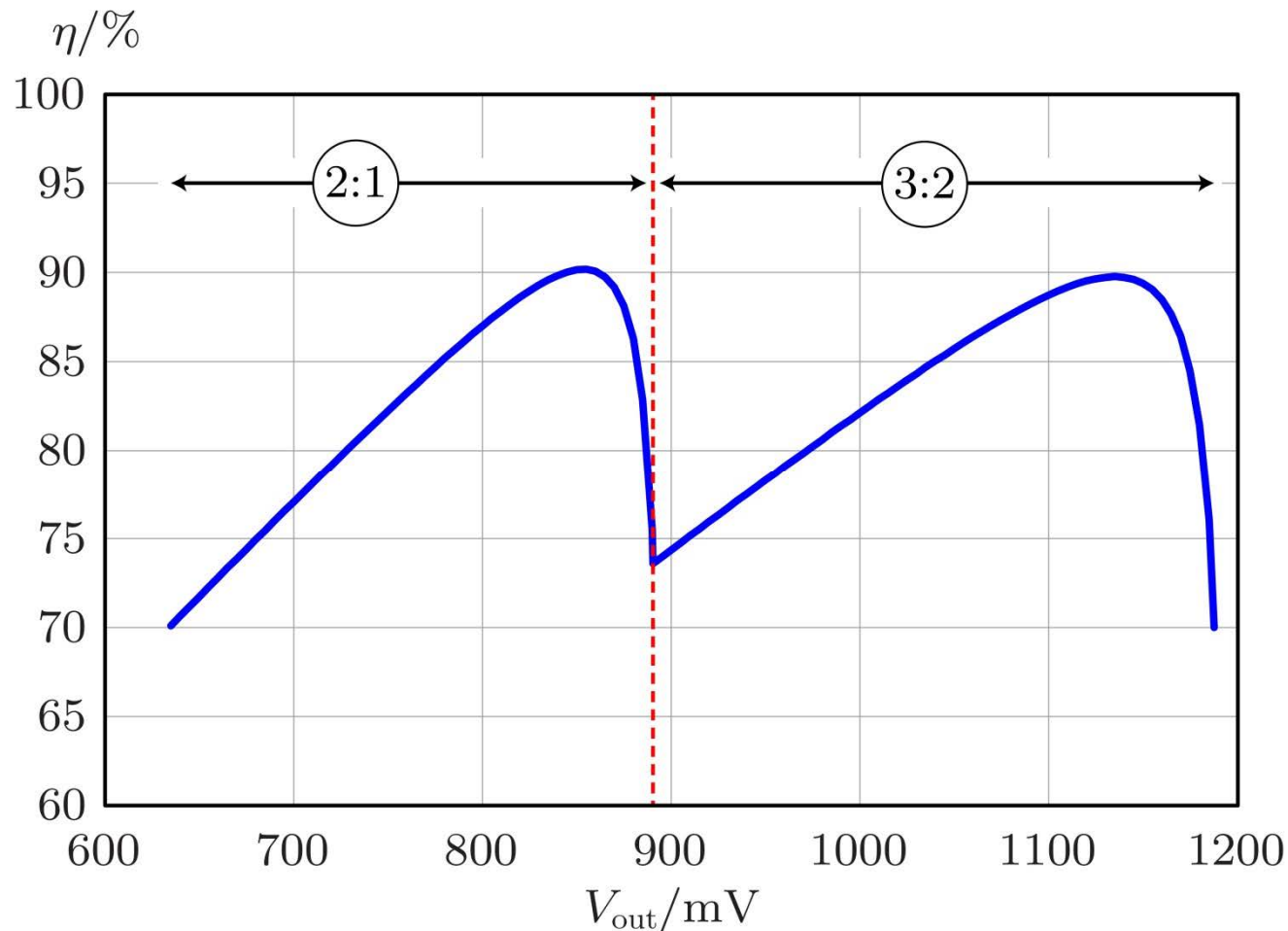
Chip overview



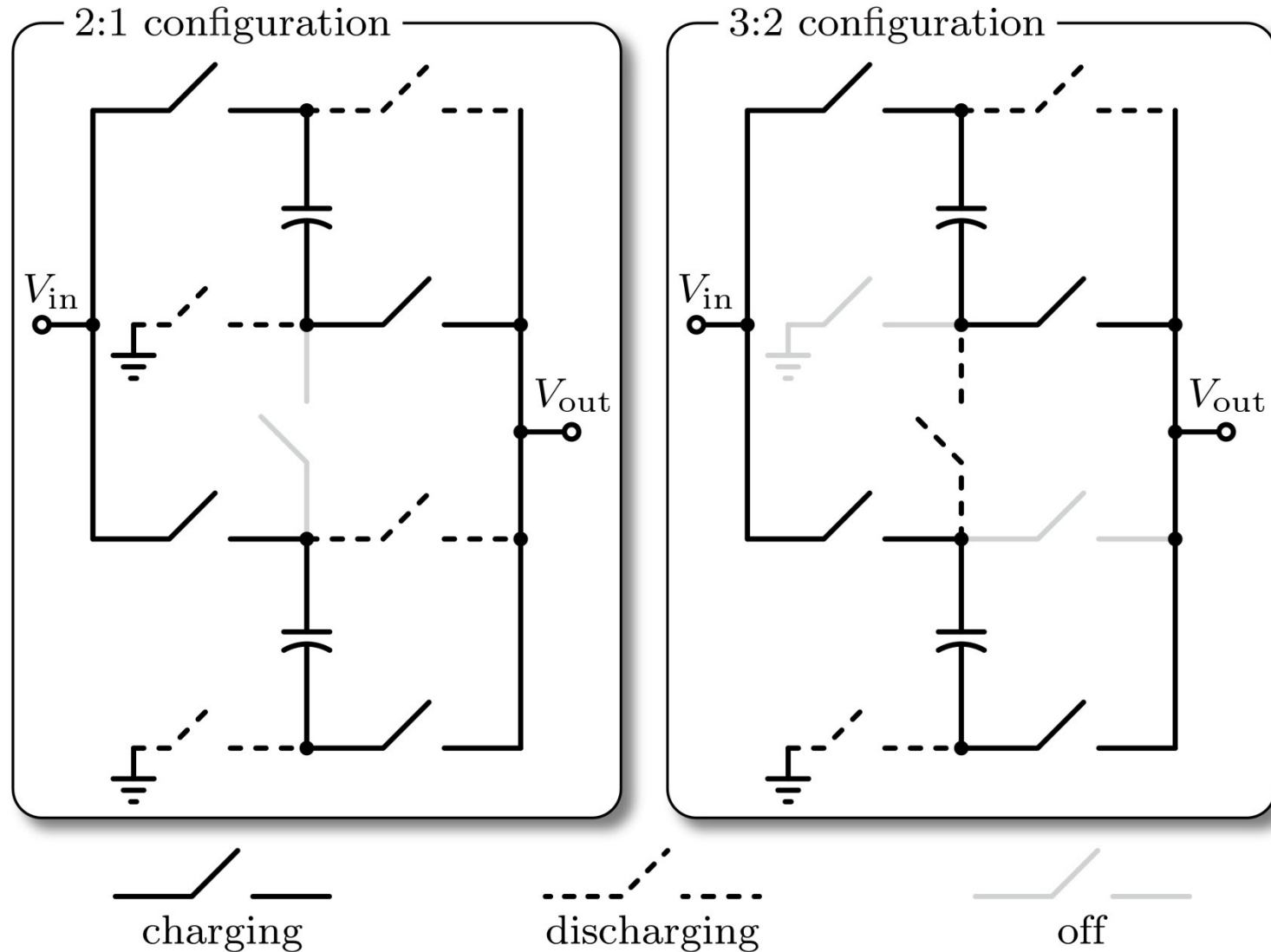
Reconfigurable SC converter

- High efficiency over a wide output voltage range

$V_{in}=1.8V$
 $f_{sw}=100MHz$

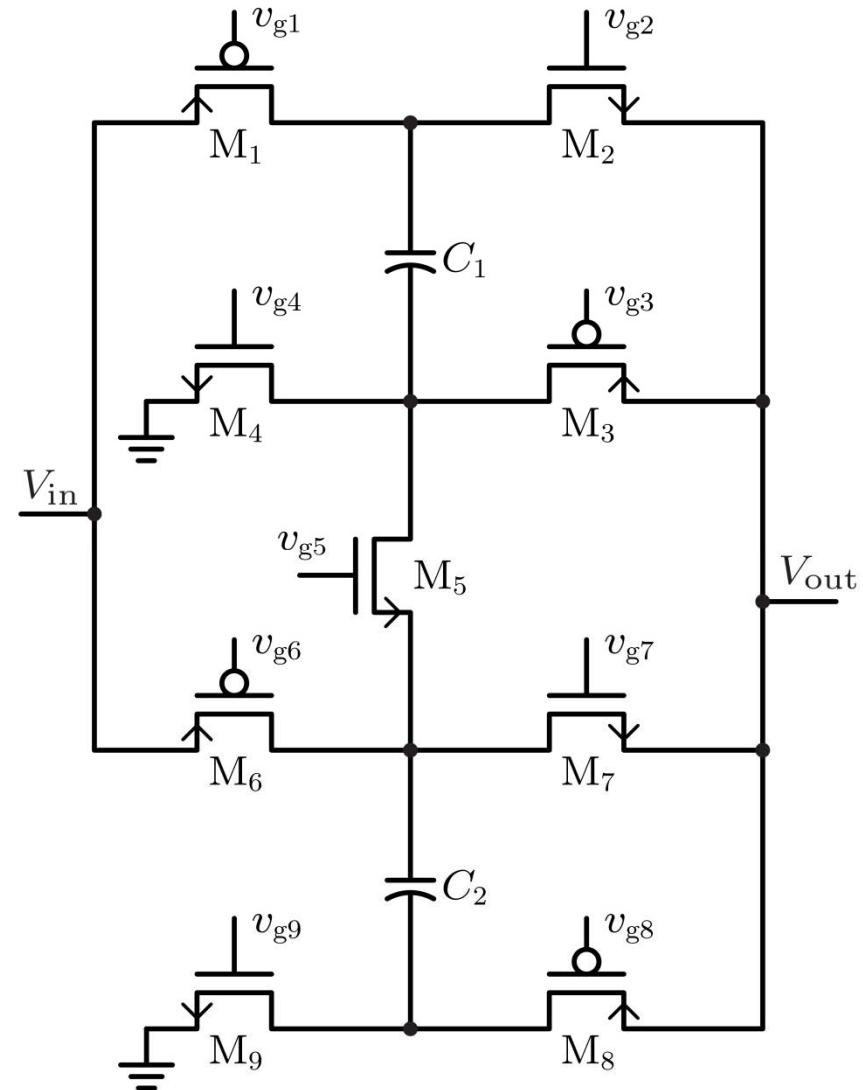
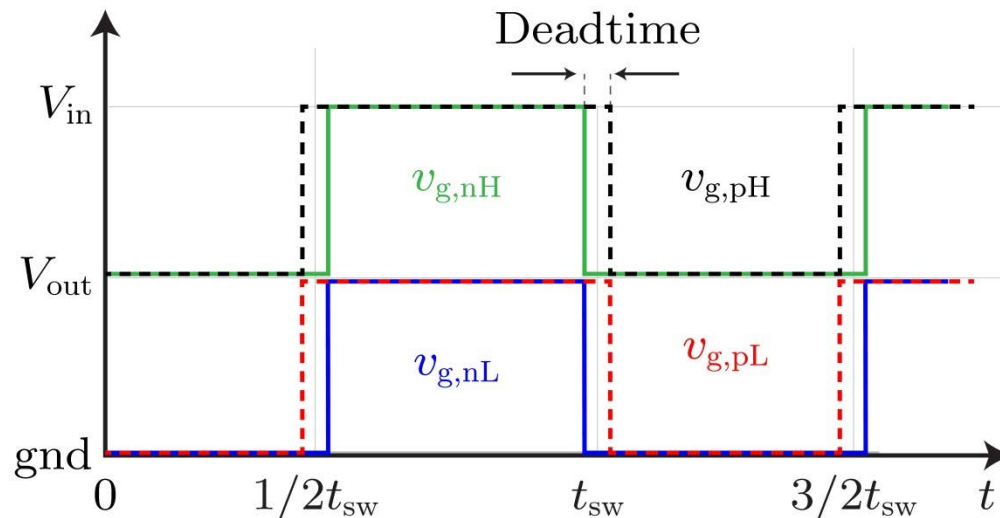


Reconfigurable SC converter power stage



Power stage: transistor implementation

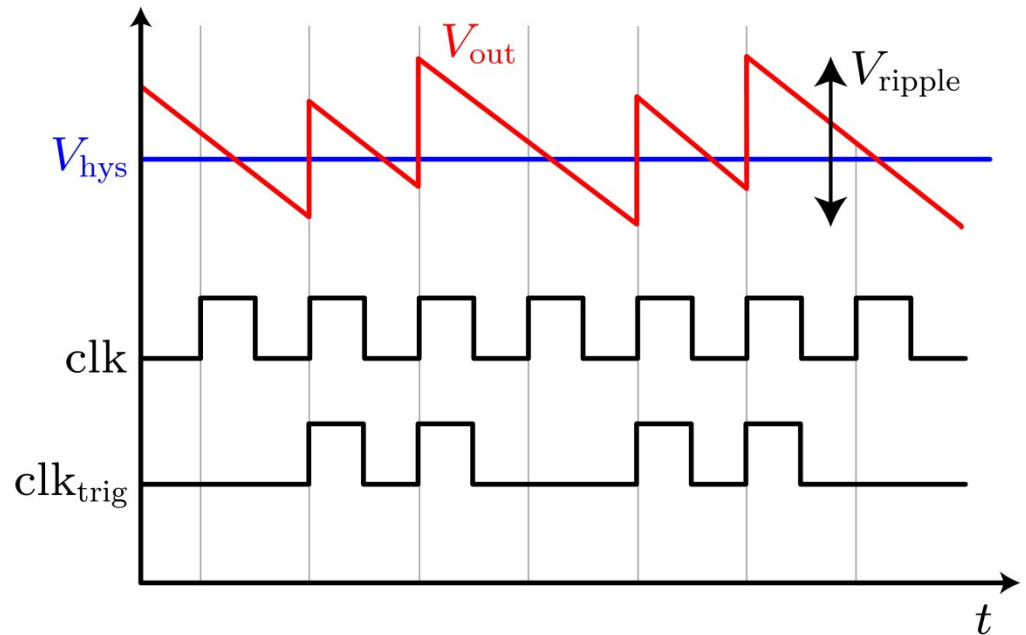
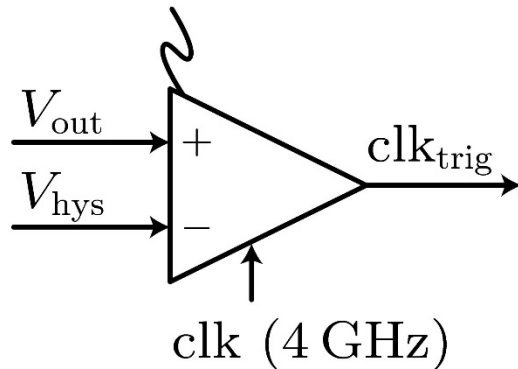
- $V_{in}=1.8V$
- $V_{block} \approx 1.2V$
- Level-shifted non-overlapping gate signals



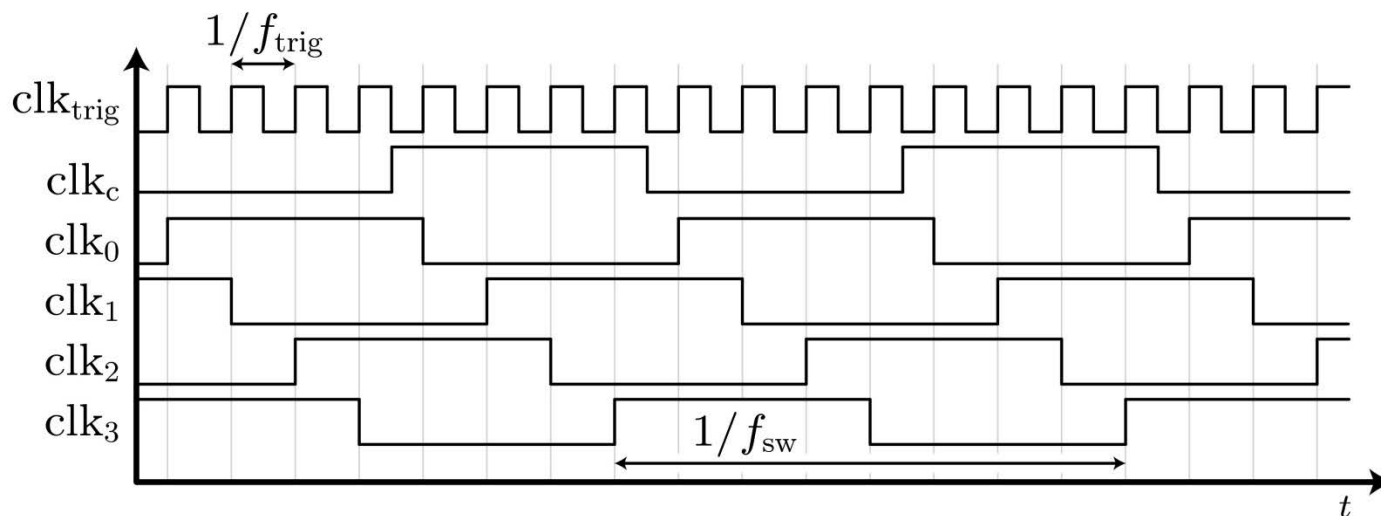
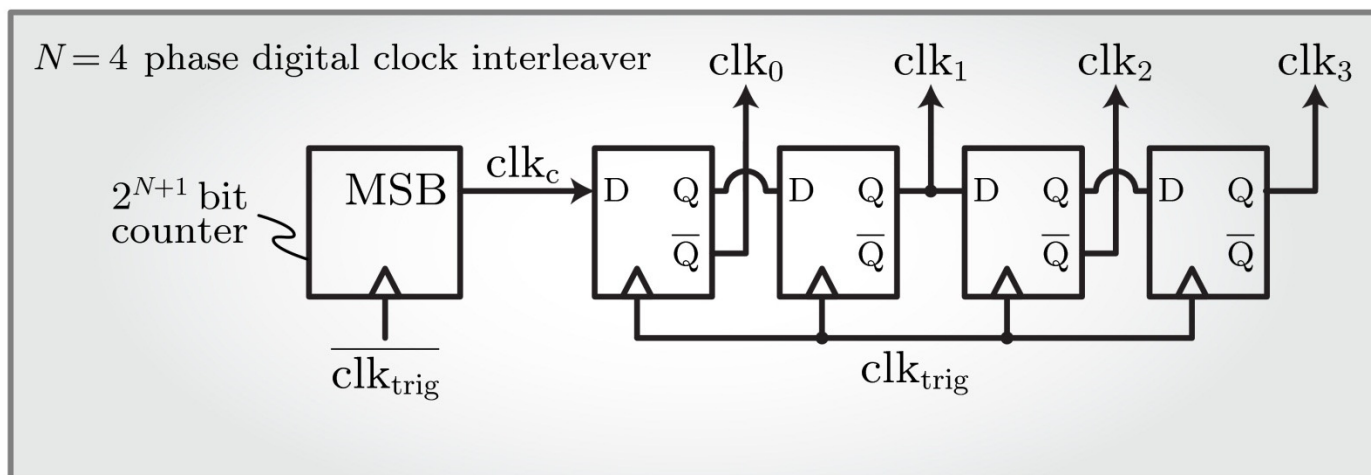
Digital controller: concept

- Single bound hysteretic control

Clocked comparator with reset



Digital controller: Clock interleaver



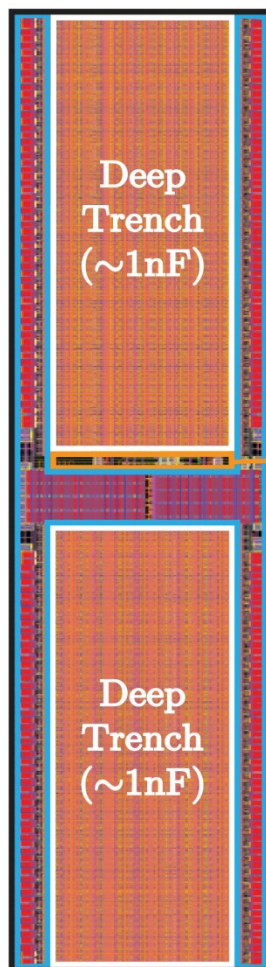
- Note: 16 phase version implemented on-chip

Implementation in 32nm SOI CMOS

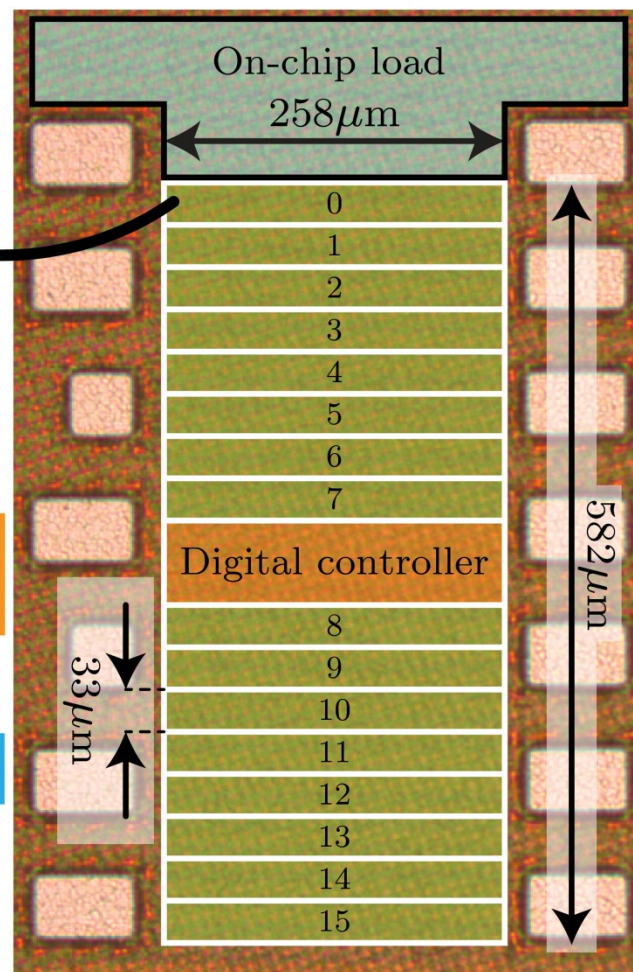
Specifications

V_{in}	= 1.8V
V_{out}	= 0.7V – 1.1V
I_{out}	= 0mA – 770mA
P_{out}	= 0mW – 840mW
C_{out}	= 0nF
# units	= 16
f_{trig}	= 4GHz
$f_{sw,max}$	= 125MHz
Area	= 0.151mm ²

SC converter unit

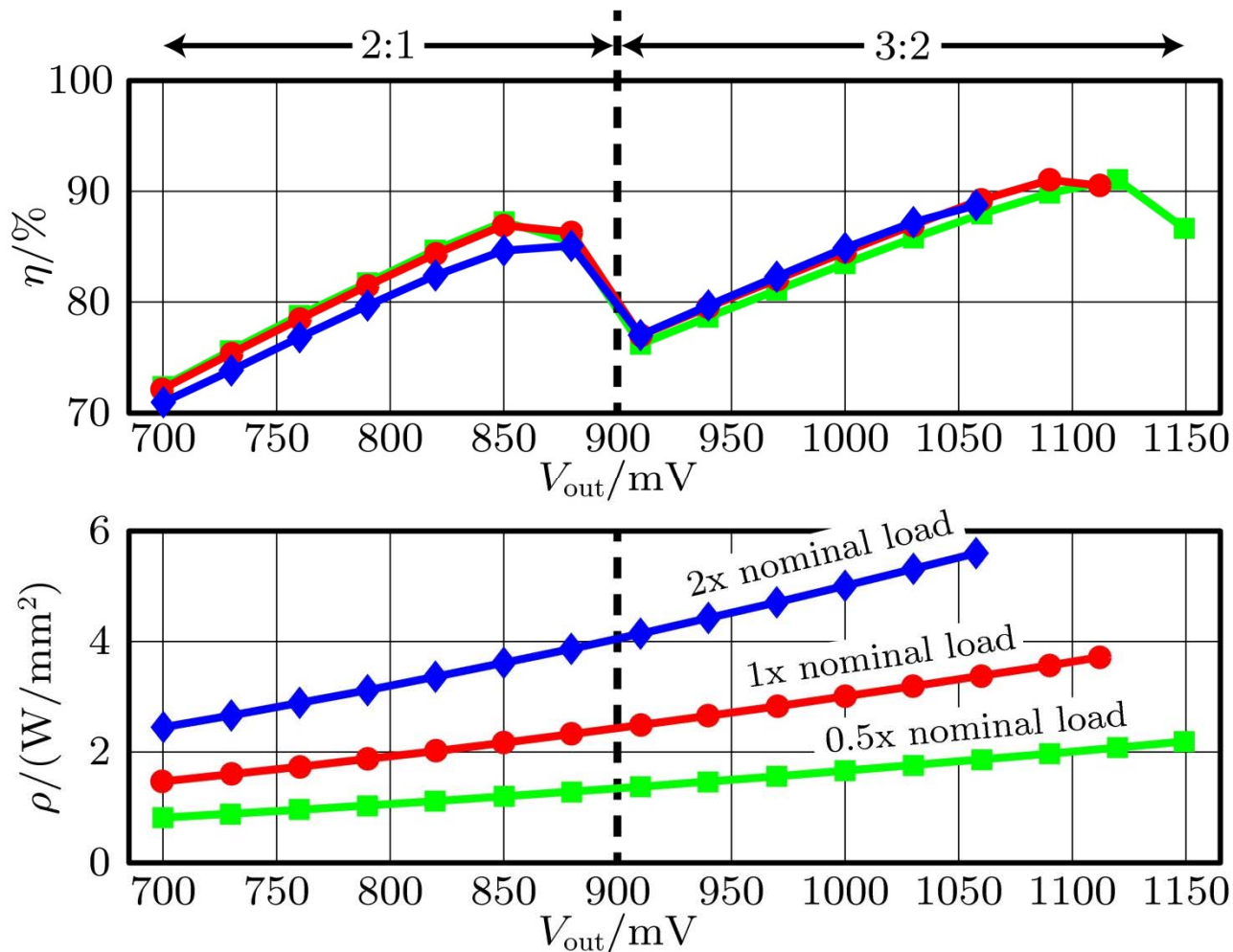


Test Chip



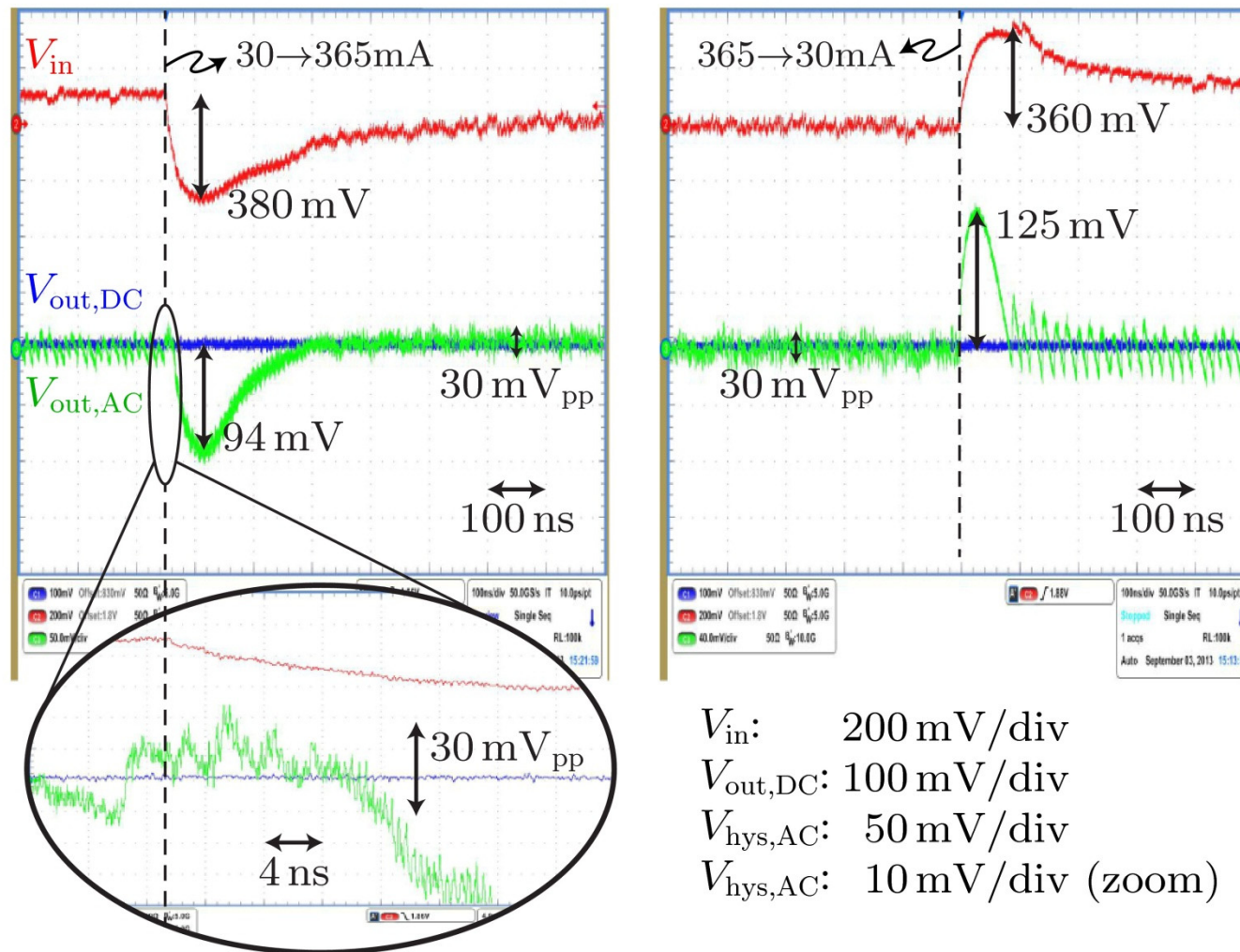
Measurement results

- Efficiency and power density



Measurement results

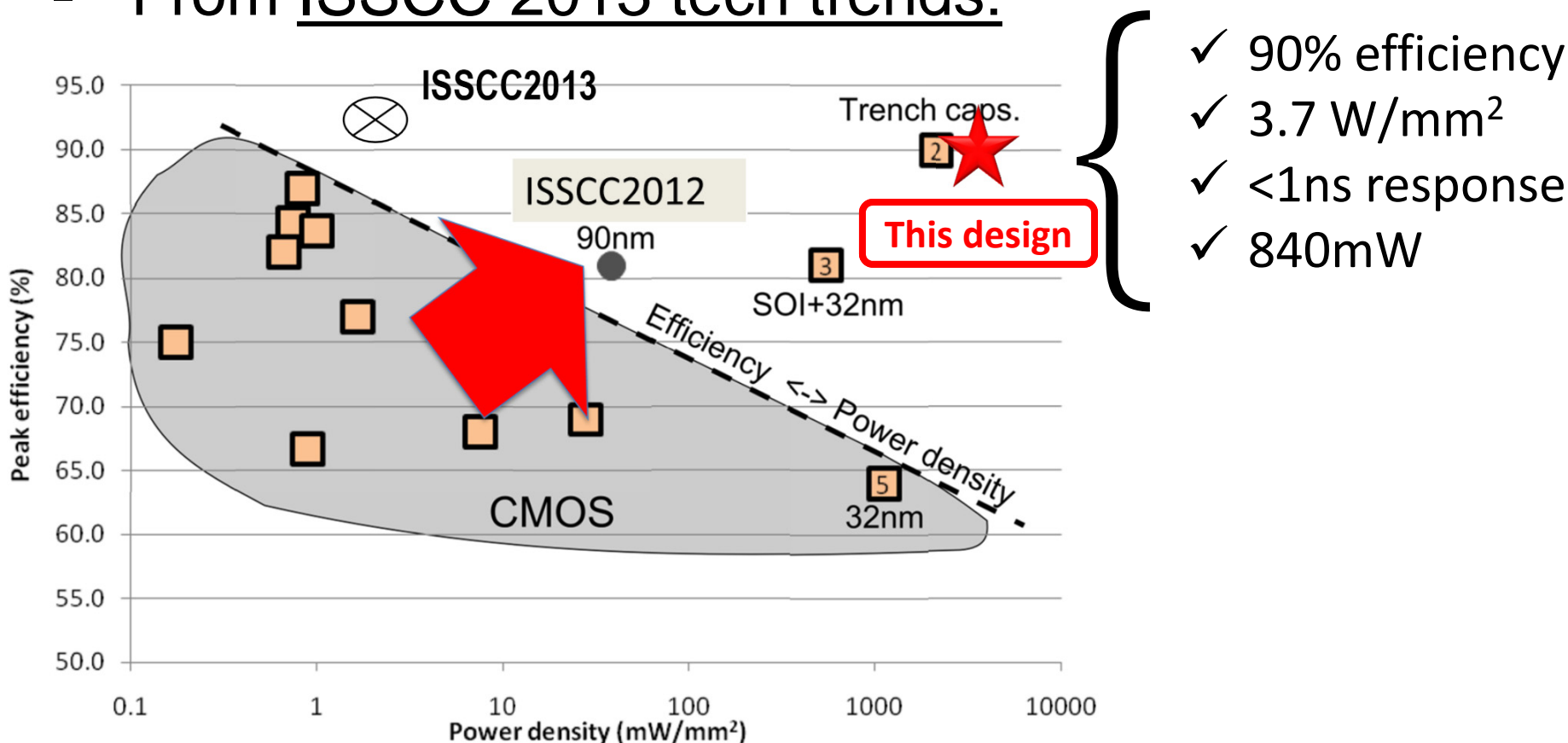
■ Transient responses



4.7: A Sub-ns Response On-Chip Switched-Capacitor DC-DC Voltage Regulator
Delivering 3.7W/mm² at 90% Efficiency using Deep-Trench Capacitors in 32nm SOI CMOS

Conclusions & comparison to prior work

- On-chip SC converter design targets:
 - High efficiency, high power density, fast response time, high power
- From ISSCC 2013 tech trends:



Paper 4.8

3-Phase 6/1 Switched-Capacitor DC-DC Boost Converter Providing 16V@7mA at 70.3% Efficiency in 1.1mm³

Ravi Karadi, Gerard Villar Piqué

NXP Semiconductors



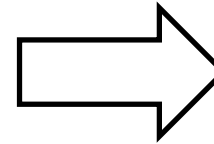
Outline

- Introduction
- 3-phase switched capacitor converter topology
- Power-plant, drivers, Controller
- Measurement results
- Conclusions

Introduction

- Applications:

OLED bias & LCD backlight supply
for mobile devices



- $V_{in} = 3.3V$
- $V_o = 16V$
- $I_o = 7mA$

- Main desired features:

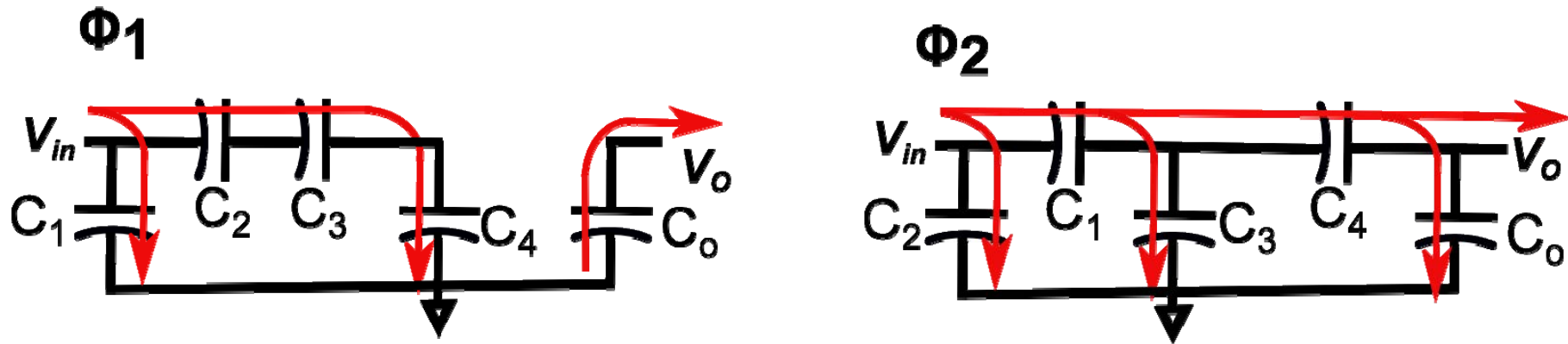
- Good efficiency
- Converter size: **small** and **thin**
- Few external components and pins

Feature	Inductive Converter	SCPC
Efficiency	Good	Good*
Size	Bulky	Small*

4.8: 3-Phase 6/1 Switched-Capacitor DC-DC Boost Converter Providing 16V@7mA at 70.3% Efficiency in 1.1mm²

At low power ~150mW

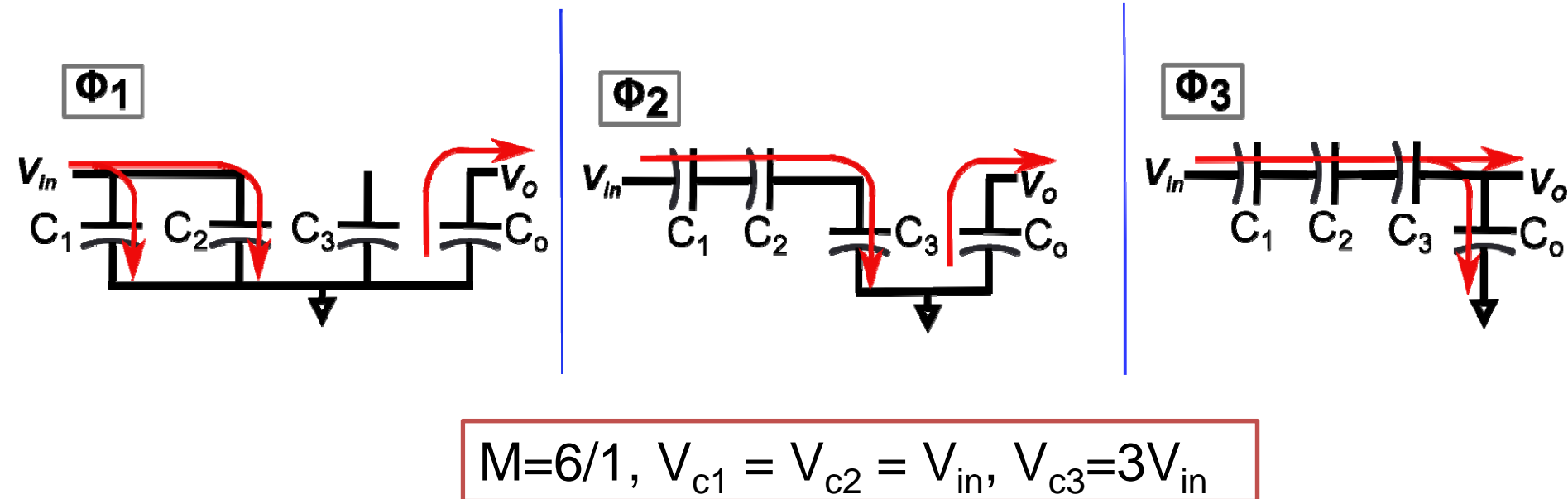
Switched-capacitor power converters (SCPC): 2 clock phases



$$M=6/1$$

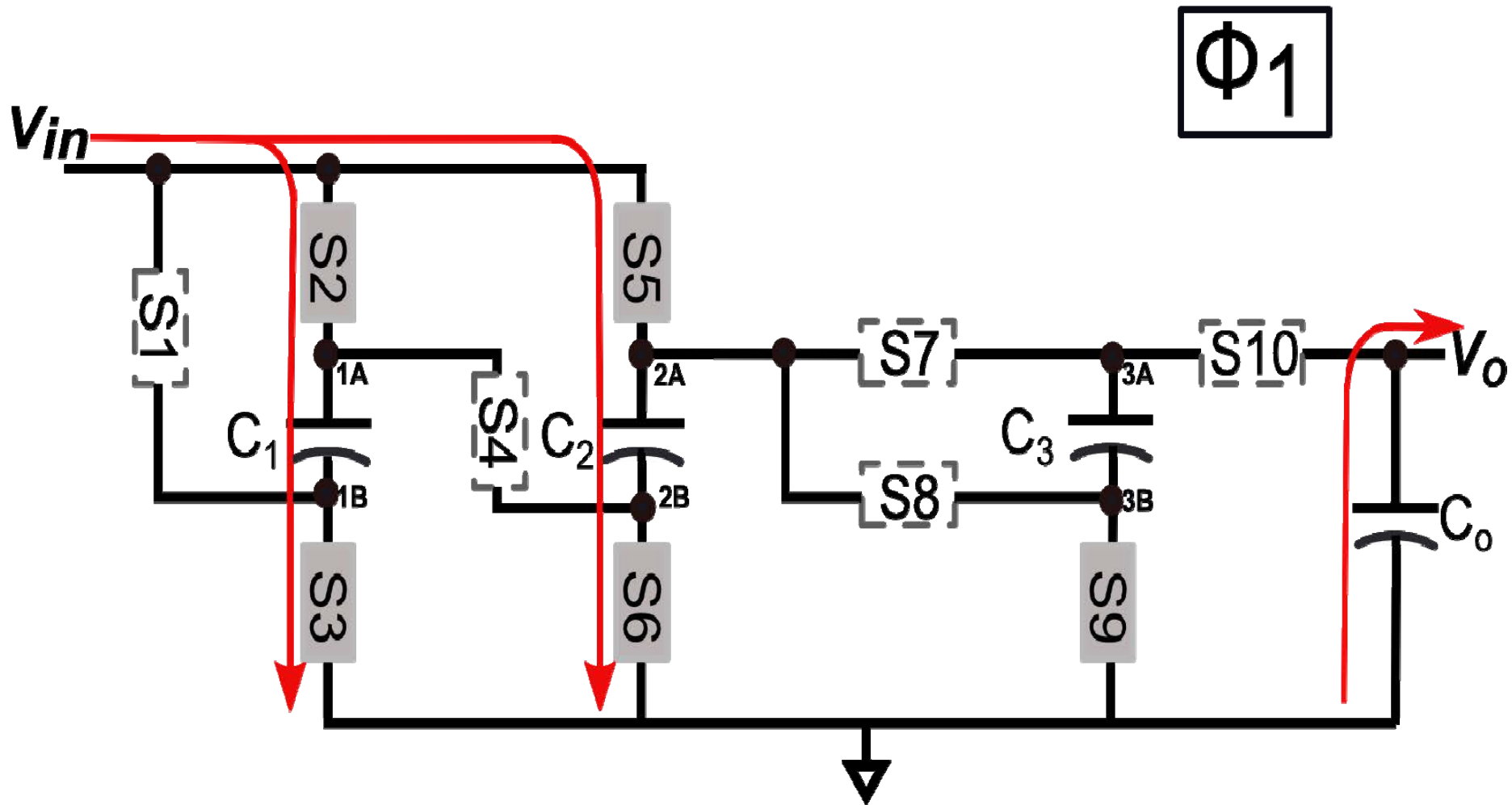
- Large number of floating capacitors and pins (e.g. 6/1 requires at least 4 floating capacitors)

3-Phase SCPC topology

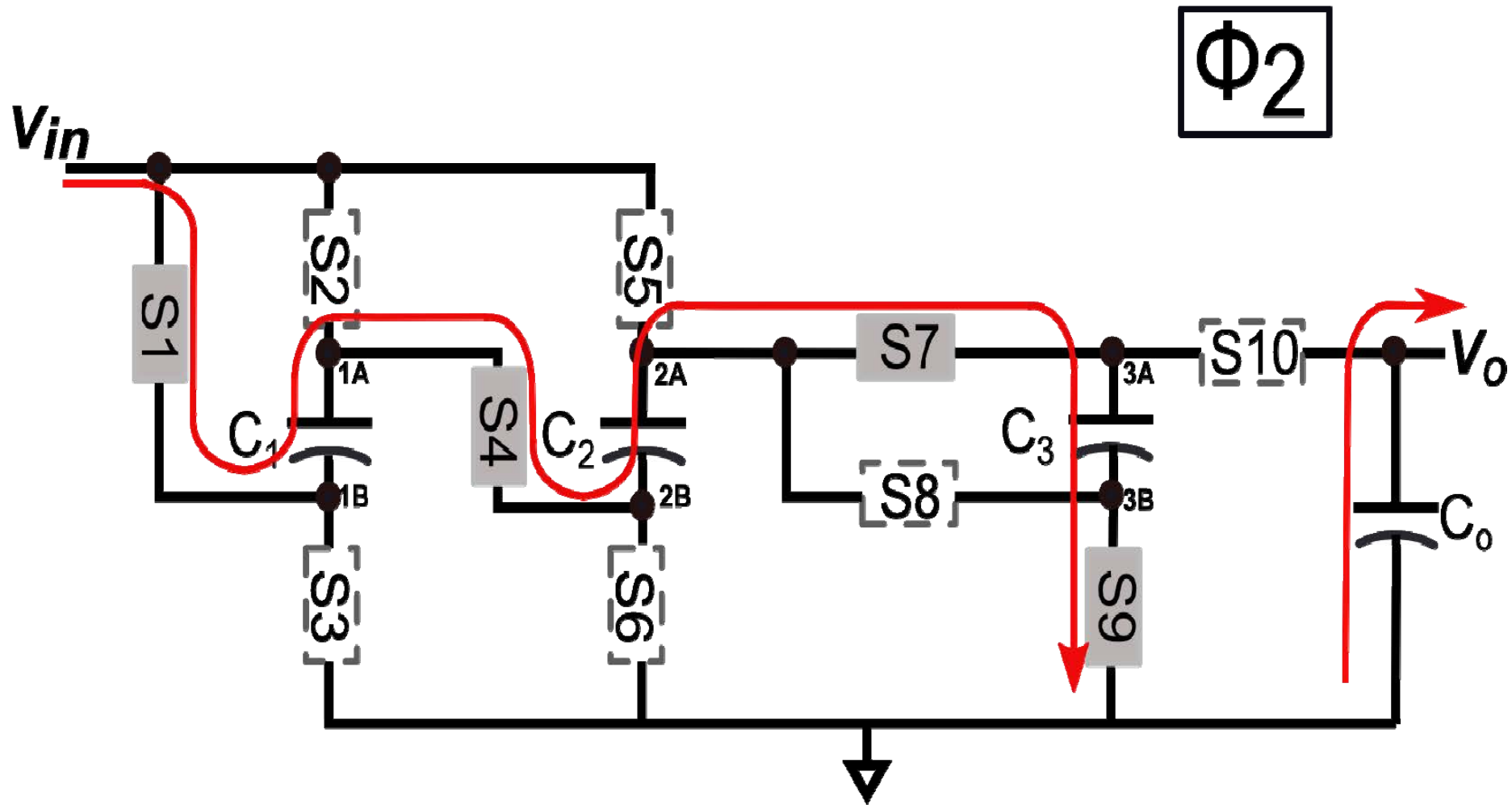


- Employs **an additional clock phase** to reduce the number of floating capacitors (**4 \rightarrow 3**)
- C_1 is integrated on chip to further reduce the external components and pins

Power plant (Φ_1)

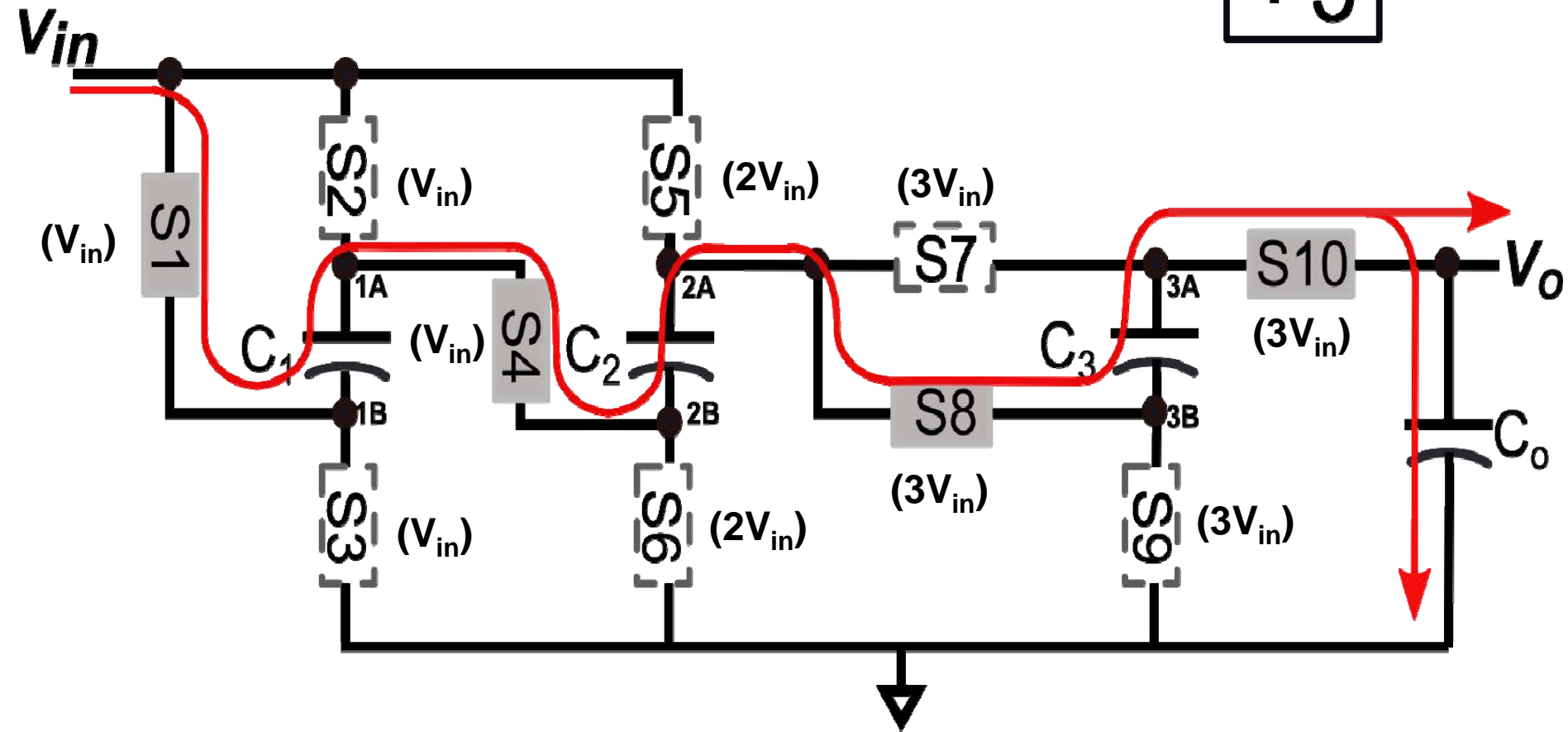


Power plant (Φ_2)

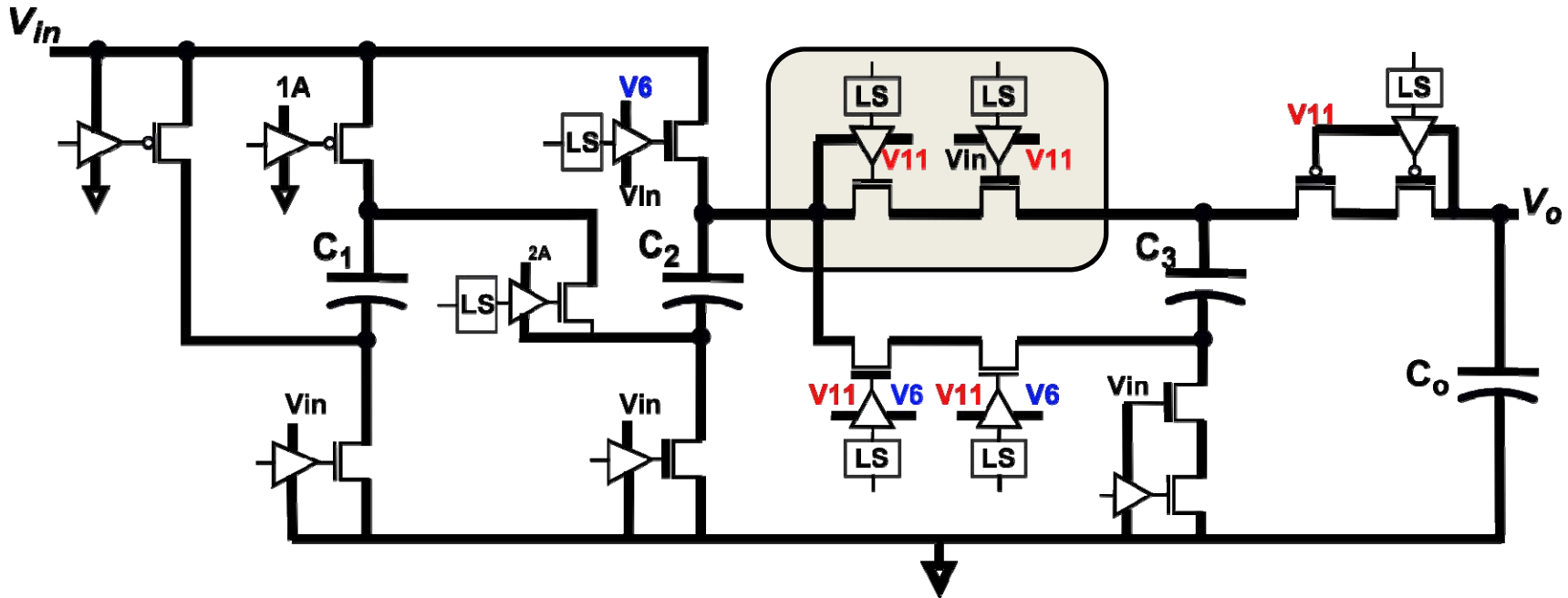


Power plant (Φ_3)

Φ_3



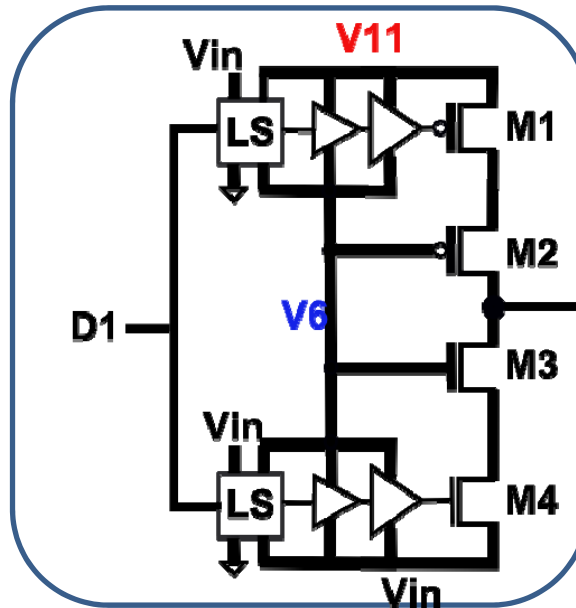
Power plant: transistor implementation



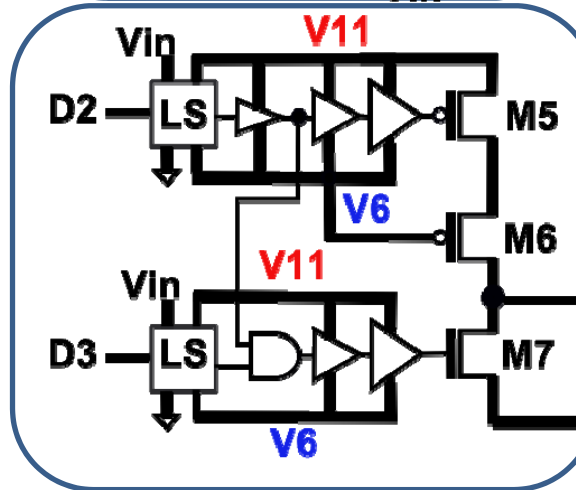
- 10 switches: single or cascode devices. Optimal size to minimize the switching losses.
- Switching at $f_{sw}=6.67\text{MHz}$ ($f_{clk}=20\text{MHz}$) to reduce the size of the capacitors
- Drivers require auxiliary rails of $V_6=5.5\text{V}$ and $V_{11}=10.5\text{V}$

Multi voltage driver

Driver 1



Driver 2



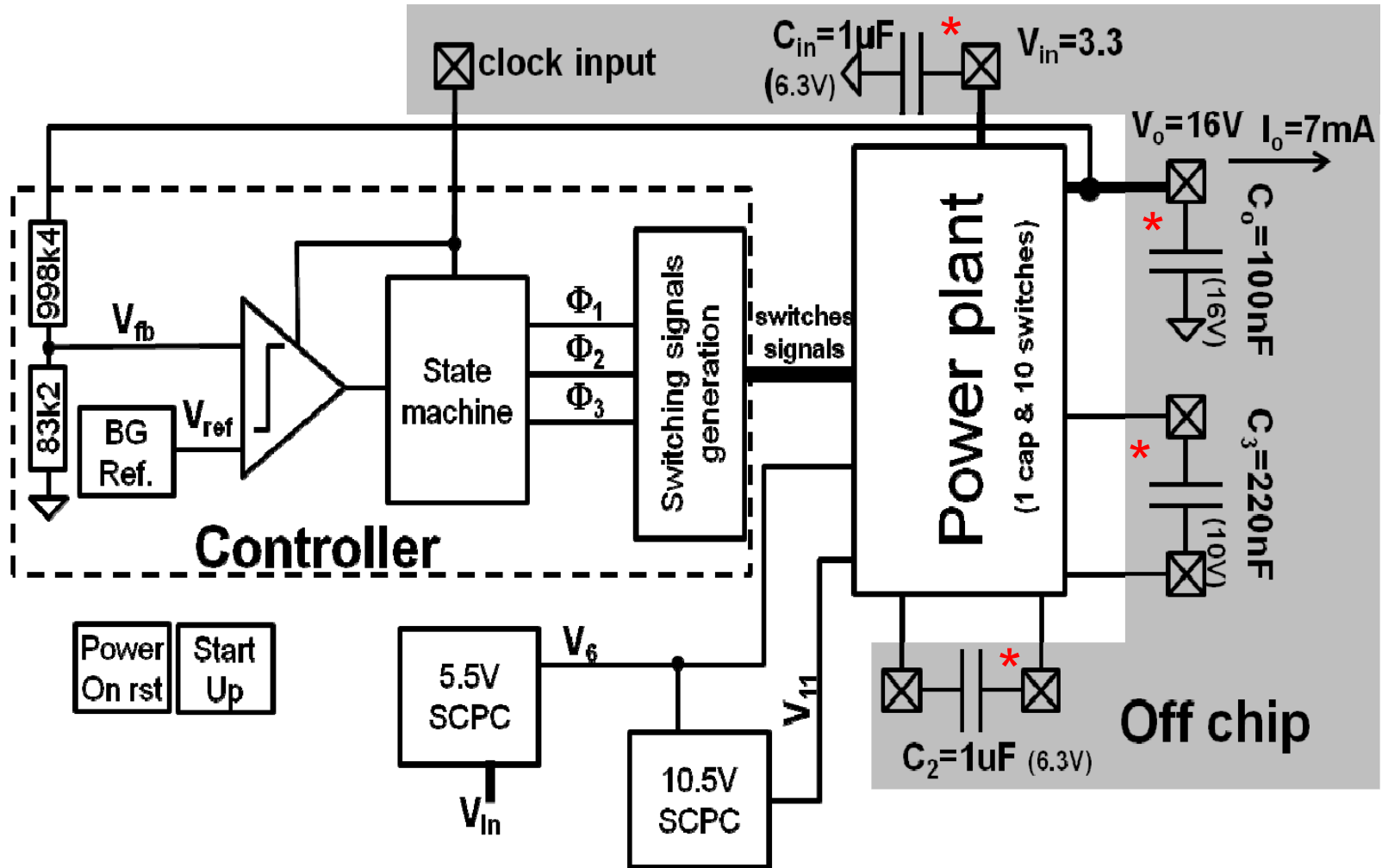
Switch S7 conducts during Φ_2

Aux. internal supply rails

■ $V_{11}=10.5V$

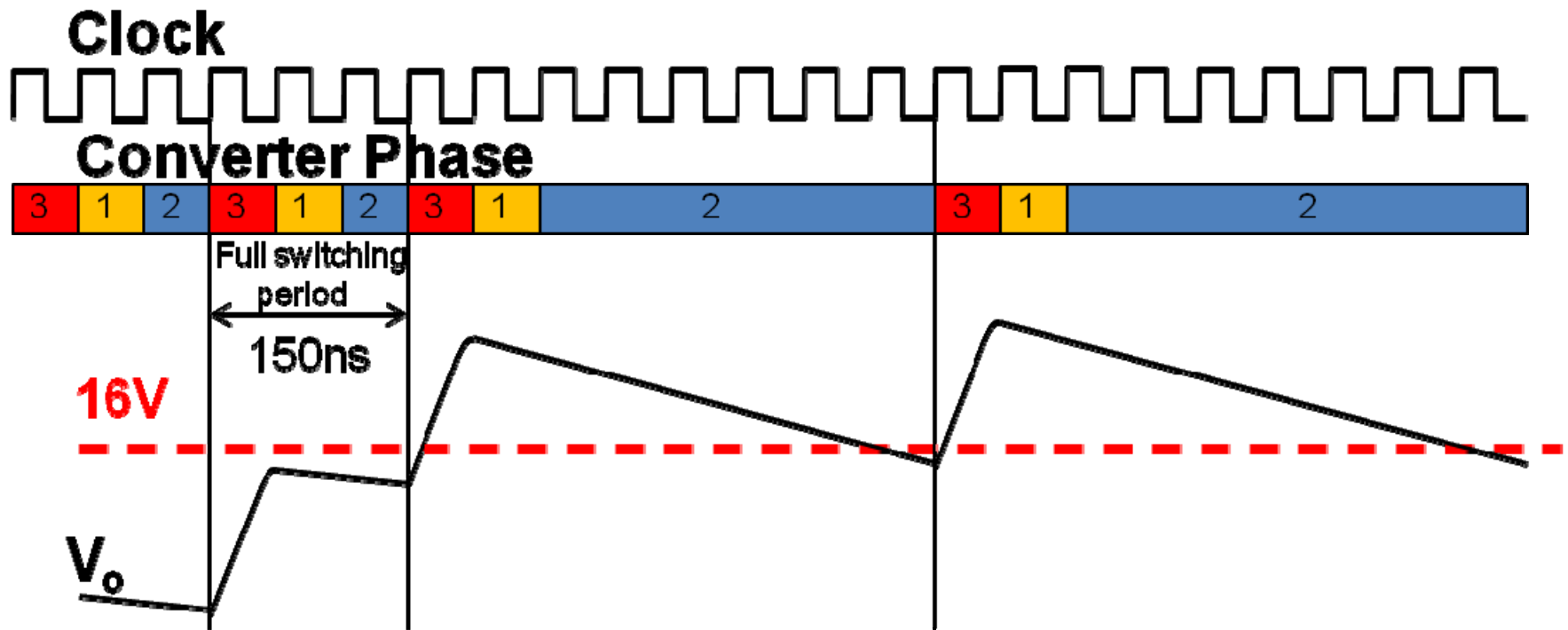
■ $V_6=5.5V$

Block diagram of the converter



* 0201 SMD capacitors

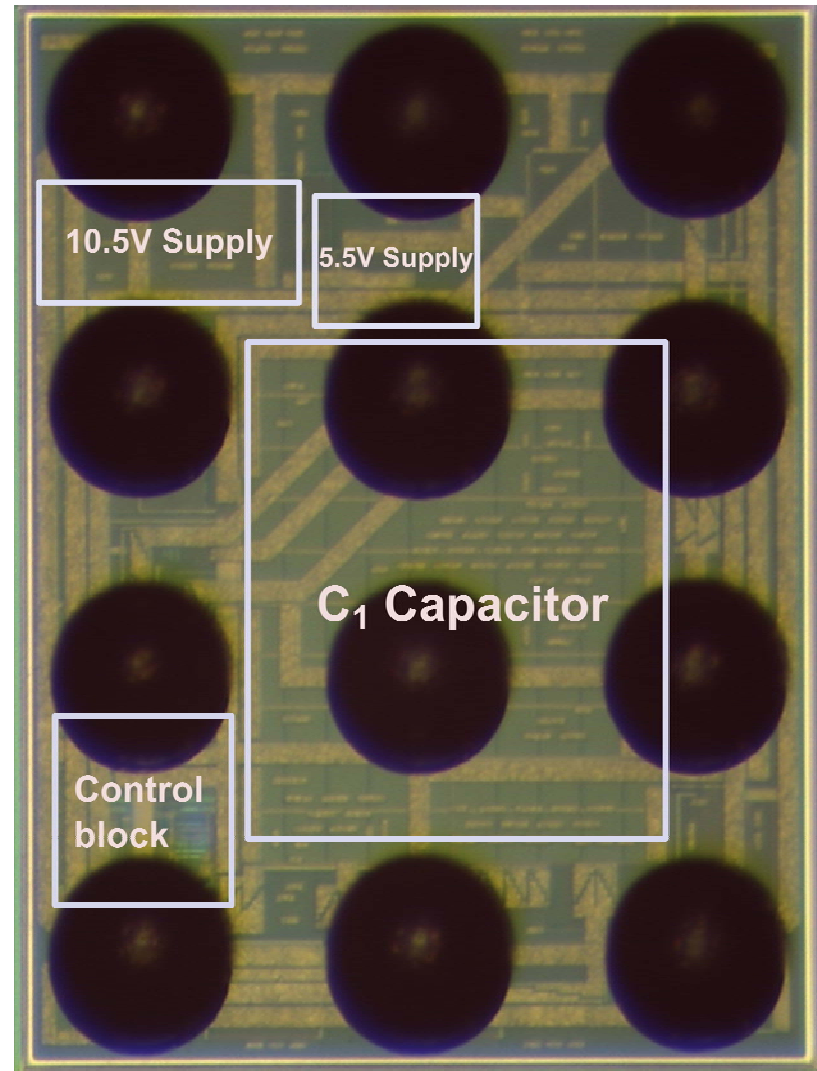
Pulse Skipping Control



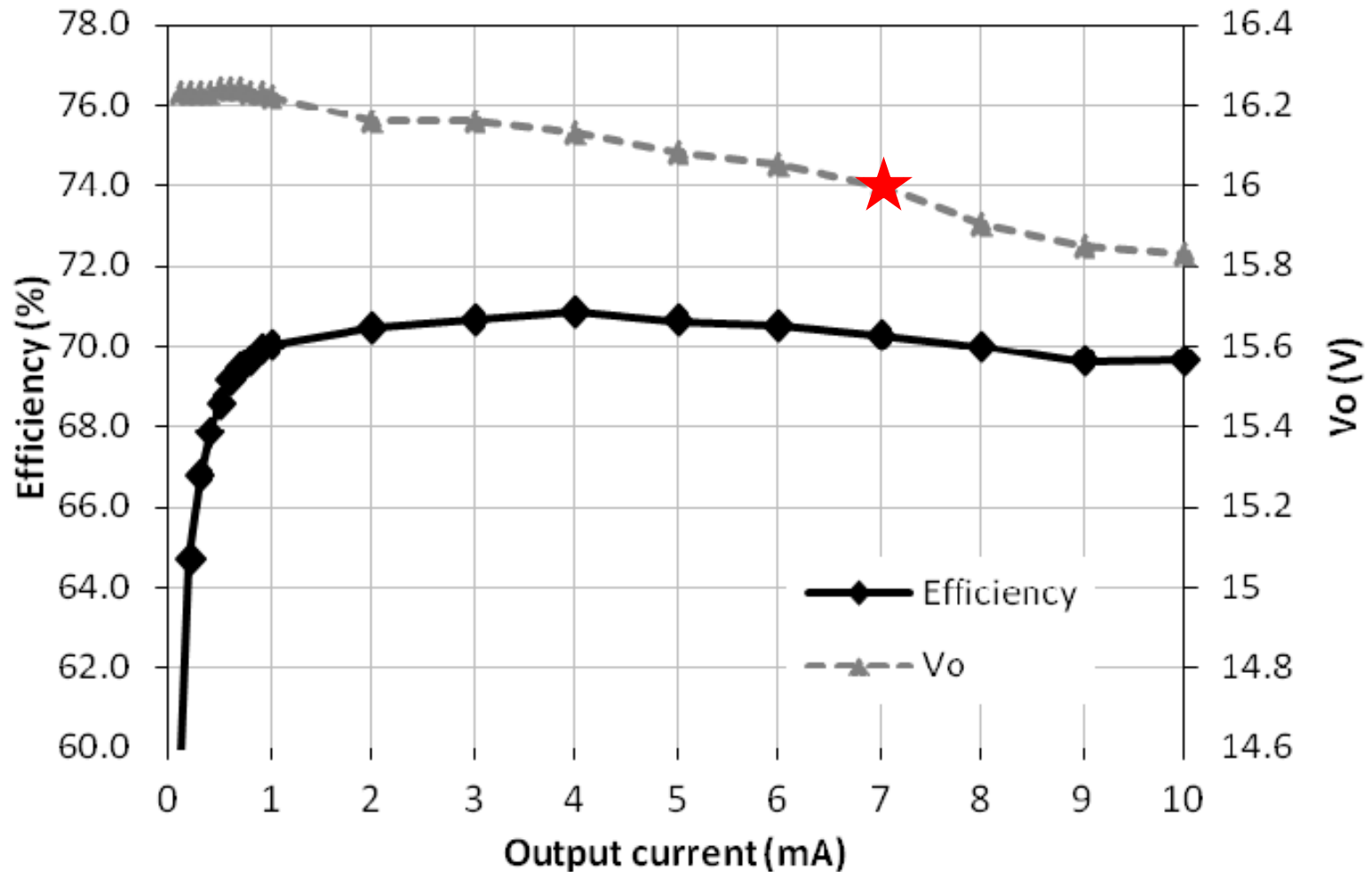
- The converter goes through Φ_1 and Φ_2 , charging the 3 floating capacitors and waits in Φ_2 while $V_o > 16V$.
- It goes to Φ_3 as soon as $V_o < 16V$ and provides charge to the output.

Test chip

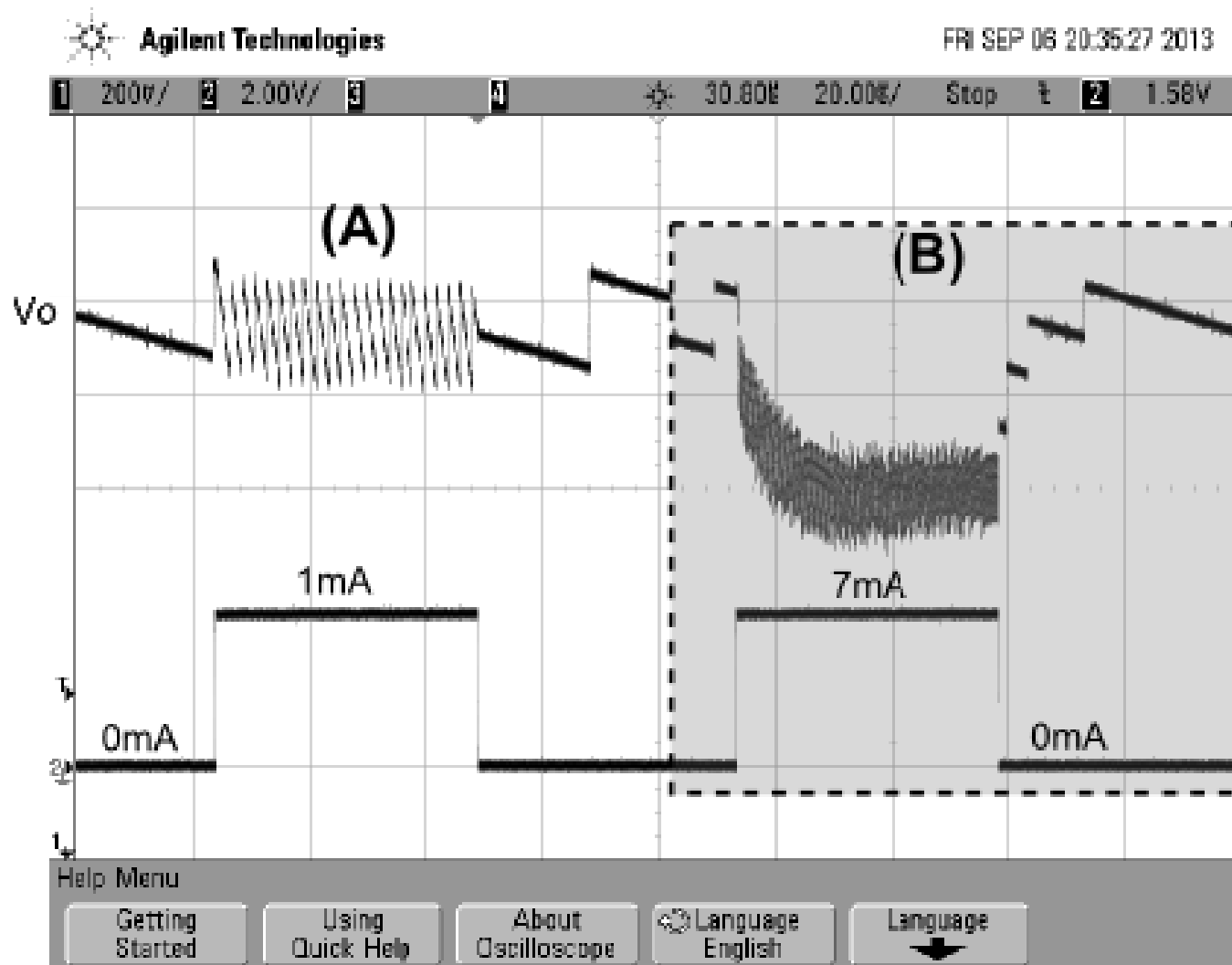
- Technology 0.16 μm CMOS
- Area = 1.65mm² (0.40mm² empty area) in a 12 bump WLCSP package
- Area of C₁ (2.3nF) = 0.45mm²



Measurement results: Efficiency



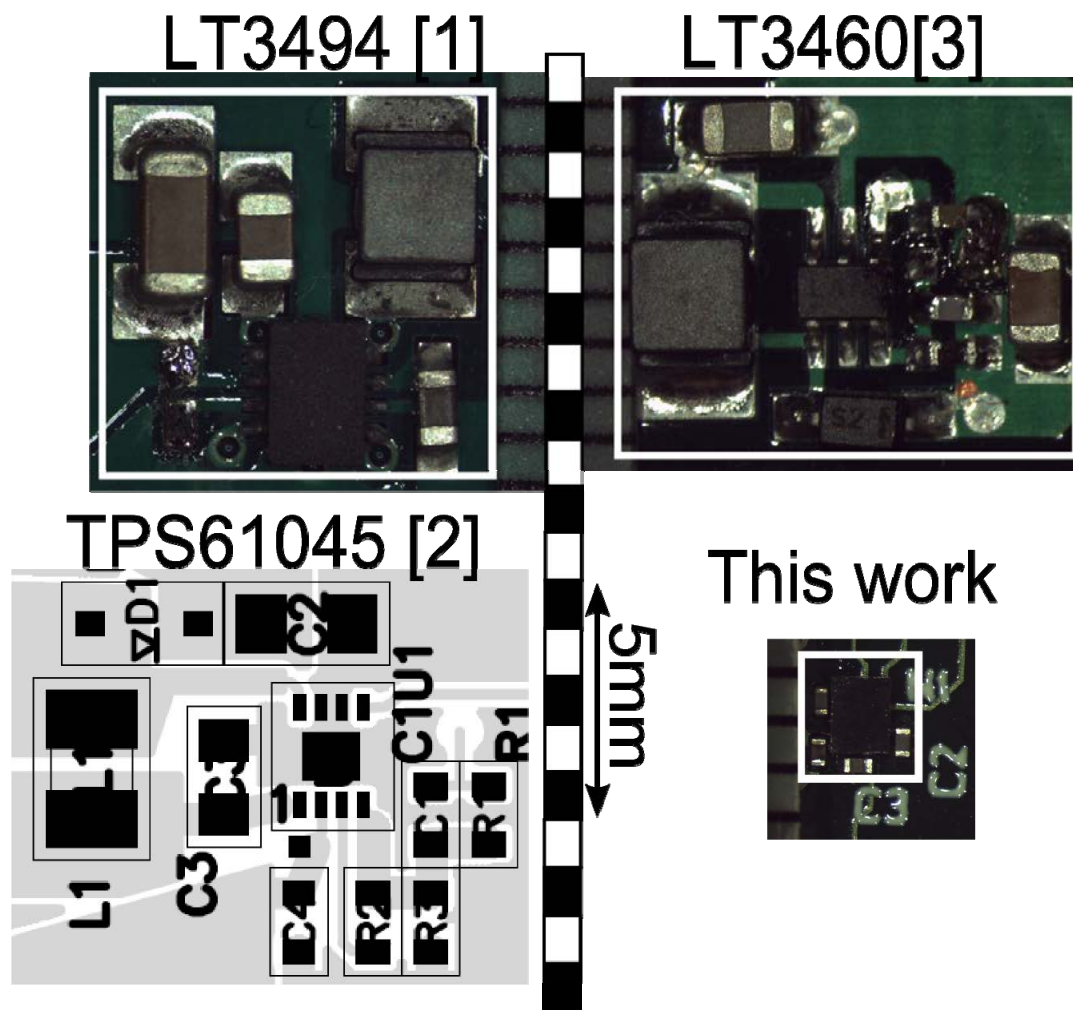
Measurement result: Step response



Benchmarking

Converter specifications	LT3494 [1]	TI TPS61045 [2]	LT3460 [3]	This work
Total Component volume (mm ³)	32	37.5	18.3	1.1
Maximum thickness (mm)	1.8	1.6	1.8	0.55
Efficiency at 16V@7mA	75.8%	84%	79%	70.3%
Efficiency at 16V@0.1mA	45.6%	--	13.2%	58.5%
Output ripple at 7mA (relative to $V_o=16V$)	0.06% ($C_o=2.2\mu F$)	0.28% ($C_o=1\mu F$)	0.3% ($C_o=1\mu F$)	1% ($C_o=100nF$)
Components	1XDFN 1x1210 2x1206 1x0603	1xOFN-8 1x1210 1x0805 1x1206 1xSOD123	1xDFN-6 1x1206 2x0603 1xSOD-323	1xWLCSP 4x0201

Comparison of PCB implementation



Conclusions

- SCPC enable extremely small form-factor solutions
- SCPC can perform on par with inductive converters at low power
- 3-Phase topology leads to reduction in number of components and pin count
- Demonstrated 3-Phase SCPC provides 7mA@16V in 1.1mm³